Design for Testability

CourseCode	23EC4702A	**Year**	IV	**Semester**	I
Course Category	PE–V	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Digital circuit design, VLSI.
ContinuousInternal Evaluation	30	**Semester End Evaluation**	70	**Total Marks**	100

Course Outcomes		
Upon successful completion of the course, the student will be able to		BL
CO1	Acquire verification knowledge and test evaluation	L4
CO2	Design for testability rules and techniques	L3
CO3	Utilize the scan architectures for different digital circuits	L4
CO4	Design of built-in-self test	L3

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3-High, 2: Medium, 1:Low)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2			2							2	
CO2	3				2							2	
CO3	3	2			2							2	
CO4	3				2							2	
Avg.	3	2			2							2	

Syllabus		
UnitNo.	**Contents**	**Mapped CO**
1	**Introduction to Testing:** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, and Faults, Levels of Fault Models, Single Stuck-at Fault.	CO1
2	**Logic and Fault Simulation**: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for Fault Simulation, ATPG.	CO2
3	**Testability Measures:** Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design.	CO3
4	**Built-In Self-Test:** The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, System, Memory BIST, Delay Fault BIST.	CO4
5	**Boundary Scan Standard:** Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Pin Descriptions.	CO3

Learning Resources	
Text Books	
1	M.L. Bushnell, V. D. Agrawal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Publishers, 2002
Reference Books	
1	M. Abramovici, M. A. Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House, 2001
2	P. K. Lala, “Digital Circuits Testing and Testability”, Academic Press,1997
e- Resources & other digital material	
1	https://nptel.ac.in/courses/117105137