DSP Processors and Architectures

CourseCode	23EC4701C	**Year**	IV	**Semester**	I
Course Category	PE–IV	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Digital Signal Processing
ContinuousInternal Evaluation	30	**Semester End Evaluation**	70	**Total Marks**	100

Course Outcomes		
Upon successful completion of the course, the student will be able to		BL
CO1	Analyze computational accuracy issues in DSP implementations.	L4
CO2	Compare different DSP processor architectures and evaluate their performance for various signal processing applications.	L5
CO3	Apply specialized addressing modes, instruction sets, and assembly-level programming in DSP processors.	L3
CO4	Analyze interfacing of various peripheral devices with DSP processors.	L4

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3-High, 2: Medium, 1:Low)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	1	2	1			1	1		2	1	1
CO2	3	3	2	2	1			1	1		2	2	1
CO3	3	2	2	1	3			1	1		2	1	1
CO4	3	3	3	2	3			1	1		2	2	2
Avg.	3	3	2	2	2			1	1		2	2	1

Syllabus		
Unit No.	**Contents**	**Mapped CO**
1	**Introduction to Digital Signal Processing:** Introduction, A Digital signal-processing system, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Digital Filters. **Computational Accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.	CO1
2	**Architectures for Programmable DSP Devices:** Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.	CO2
3	**Programmable Digital Signal Processors:** Commercial digital signal processing devices, Data Addressing modes of TMS320C54XX Processors, Memory space, Program Control, TMS320C54XX instructions and programming, On-Chip Peripherals, Interrupts and Pipeline operation of TMS320C54XX Processors.	CO3

4	**Analog Devices Family of DSP Devices:** ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP2181 high performance processor. Introduction to Blackfin Processor, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.	CO2
5	**Interfacing Memory and I/O Peripherals to Programmable DSP Devices:** Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).	CO4

Learning Resources
Text Books
1. Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004. 2. K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, A Practical Approach to Digital Signal Processing, New Age International, 2006/2009.
Reference Books
1. B. Venkataramani and M. Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, Tata McGraw Hill, 2004. 2. Lapsley et al., DSP Processor Fundamentals: Architectures & Features S. Chand & Co., 2000. 3. Amy Mar, Digital Signal Processing Applications using the ADSP-2100 Family by the Applications Engineering Staff of Analog Devices, DSP Division, PHI
e- Resources & other digital material
1. https://ocw.snu.ac.kr/node/25239 2. https://nptel.ac.in/courses/108106149