VLSI Design

Course Code	23EC3601	**Year**	III	**Semester**	II
Course Category	PC	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Switching Theory and Logic Design
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes		
Upon successful completion of the course, the student will be able to		**BL**
CO1	Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.	L2
CO2	Design basic building blocks in Analog IC design	L4
CO3	Design various CMOS logic circuits for design of Combinational and Sequential logic circuits.	L4
CO4	Analyze the behavior of static and dynamic logic circuits	L4
CO5	Apply various Programmable Logic Devices	L3

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)
Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

COs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PSO1**	**PSO2**
CO1	3				2						1	3	
CO2	3	2			2						1	3	
CO3	3	2			2						1	3	
CO4	3	2			2						1	3	
CO5	3				2						1	3	
Avg.	3	2			2						1	3	

	Syllabus	
Unit No	**Contents**	**Mapped CO**
1	**Introduction and Basic Electrical Propertiesof MOS Circuits:** VLSI Design Flow, Introduction to IC technology, Fabrication process: nMOS, CMOS. I_{ds} versus V_{ds} MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, The CMOS Inverter, Comparison between CMOS and BiCMOS technology,	**CO1**
2	**Basic Circuit Concepts:** Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, **Scalingof MOS Circuits:** Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density.	**CO1**
3	**Basic Building Blocks of Analog IC Design:** Common Source amplifier,	**CO2,CO3**

	Common Drain amplifier **MOS Circuit Design Process:** MOS Layers, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits	
4	**CMOS Combinational and Sequential Logic Circuit Design:** **Static CMOS Design:** Complementary CMOS, Pass-Transistor Logic, design of Half adder, full adder. **Dynamic CMOS Design:** Principle of Dynamic Logic-Domino Logic, Dynamic D Latch	**CO3,CO4**
5	**FPGA Design:** FPGA design flow, Basic FPGA architecture, FPGA Technologies. **Introduction to Advanced Technologies:** GaAs, GaN Technologies, Principles of FinFET.	**CO5**

Learning Resources
Text Books
1. Douglas A. Pucknell, Kamran Eshraghian,Essentials of VLSI Circuits and Systems, 1 st Ed., Prentice Hall, 2012. **2.** Behzad Razavi,Design of Analog CMOS Integrated Circuits , McGraw Hill, 2003
References
1. John P. Uyemura, John Wiley &Sons,Introduction to VLSI Circuits and Systems, reprint 2009. 2. Vinod Kumar Khanna,IntegratedNanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies,Springer India, 1st edition, 2016. 3. ColingeJP, FinFETs and other multi-gate transistors, Editor New York, Springer,2008.
e-Resources
1. https://nptel.ac.in/courses/108/107/108107129/ **2.** https://www.cin.ufpe.br/~mel/pub/prototipac%E3o/referencias/CMOS_design/CMOS-VLSI-design.pdf