

Code: 23EC3602

**III B.Tech - II Semester - Regular Examinations – APRIL 2026****MICROPROCESSORS & MICROCONTROLLERS  
(ELECTRONICS & COMMUNICATION ENGINEERING)**

Duration: 3 hours

Max. Marks: 70

- Note: 1. This question paper contains two Parts A and B.  
 2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.  
 3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.  
 4. All parts of Question paper must be answered in one place.

BL – Blooms Level

CO – Course Outcome

**PART – A**

		BL	CO
1.a)	List different types of interrupts in 8086.	L1	CO1
1.b)	Discuss the role of queue in 8086 architecture.	L2	CO1
1.c)	What is the function of the Debug system in Cortex-M?	L1	CO1
1.d)	Explain register set in Cortex-M architecture.	L2	CO1
1.e)	Explain any two assembler directives in Cortex-M.	L2	CO1
1.f)	List different data processing instructions in Cortex-M.	L1	CO1
1.g)	Discuss the steps to configure a microcontroller pin as input and output.	L2	CO1
1.h)	Define GPIO in a Cortex-M based microcontroller.	L1	CO1
1.i)	Discuss the need for timing interfaces in real-time applications.	L2	CO1
1.j)	Why is frequency pre-scaling required?	L2	CO1

## PART – B

			BL	CO	Max. Marks
<b>UNIT-I</b>					
2	a)	Explain assembly language development tools.	L1	CO1	5 M
	b)	Compare minimum mode and maximum mode configuration.	L2	CO1	5 M
<b>OR</b>					
3	a)	Explain various addressing modes with examples.	L3	CO2	5 M
	b)	Develop an assembly language program to add two 16-bit numbers.	L3	CO2	5 M
<b>UNIT-II</b>					
4	a)	Describe the bus system and bus matrix organization in Cortex-M.	L3	CO2	5 M
	b)	Describe interrupt configuration in Cortex-M.	L3	CO2	5 M
<b>OR</b>					
5	a)	Explain exception handling mechanism in Cortex-M.	L3	CO2	5 M
	b)	Differentiate between Cortex-M and 8086 with respect to architectures.	L3	CO2	5 M
<b>UNIT-III</b>					
6	a)	Demonstrate LDR and STR memory access instructions.	L3	CO2	5 M
	b)	Illustrate various Data Processing instructions in Cortex-M.	L3	CO2	5 M
<b>OR</b>					

7	a)	Demonstrate 16 bit instruction encoding in Cortex-M.	L3	CO2	5 M
	b)	Demonstrate the execution flow of a loop using branch instructions.	L3	CO2	5 M
<b>UNIT-IV</b>					
8	a)	Analyze LED and switch interfacing with Cortex-M with neat diagram.	L4	CO3	5 M
	b)	Compare and contrast serial communication and parallel communication in UART.	L4	CO3	5 M
<b>OR</b>					
9	a)	Analyze how to interface a seven segment display and TM4C123 microcontroller.	L4	CO3	5 M
	b)	Analyze how to configure ADC for analog input conversion.	L4	CO3	5 M
<b>UNIT-V</b>					
10	a)	Analyze basic timing interfaces in TM4C123 microcontroller.	L4	CO3	5 M
	b)	Evaluate the generation of pulse width modulation using timer as an output device.	L5	CO4	5 M
<b>OR</b>					
11	a)	Analyze the working of SysTick Timer in TM4C123 microcontroller.	L4	CO3	5 M
	b)	Design the steps to generate variable frequency signals using timers.	L5	CO4	5 M