PVP 23

Code: 23EC3601

III B.Tech - II Semester - Regular Examinations – APRIL 2026

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO
1.a)	Define output conductance (g_{ds}) in a MOS transistor.	L1	CO1
1.b)	What is channel length modulation?	L1	CO1
1.c)	How does scaling affect subthreshold leakage?	L2	CO1
1.d)	How does sheet resistance affect nMOS inverter?	L2	CO1
1.e)	A CS amplifier has gm = 2 mS and RD = 10 kΩ. Determine the voltage gain.	L3	CO2
1.f)	State the objective of preparing a stick diagram.	L1	CO3
1.g)	If VDD = 3.3 V and VT = 0.7 V, find output high level after one NMOS pass transistor.	L3	CO3
1.h)	Why is static power dissipation low in CMOS circuits?	L2	CO4
1.i)	What is the difference between simulation and synthesis in FPGA design?	L2	CO5

1.j)	Why is GaN suitable for high-power applications?	L2	CO5

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	With a neat circuit diagram, explain the operation of an nMOS inverter.	L2	CO1	5 M
	b)	Sketch and explain the Voltage Transfer Characteristics (VTC) of CMOS inverter.	L2	CO1	5 M
		OR			
3	a)	Interpret the drain current equation for MOS transistor in saturation.	L2	CO1	6 M
	b)	Differentiate between COMS and Bi-COMS technology.	L2	CO1	4 M
		UNIT-II			
4	a)	Describe the relation between resistivity and sheet resistance.	L2	CO1	6 M
	b)	Explain how sheet resistance applied for MOS circuits.	L2	CO1	4 M
		OR			
5	a)	Discuss the scaling factors for device parameters.	L2	CO1	7 M
	b)	Explain scaling limitation of current density.	L2	CO1	3 M

UNIT-III					
6	a)	Define a Common Drain amplifier with circuit diagram.	L1	CO2	3 M
	b)	Derive the voltage gain expression of Common Drain amplifier.	L4	CO2	7 M
OR					
7	a)	Explain lambda-based design rules.	L2	CO3	7 M
	b)	State advantages of λ-based methodology.	L2	CO3	3 M
UNIT-IV					
8	a)	Define Pass-Transistor Logic and explain its operating principle.	L1	CO3	4 M
	b)	Implement a Half Adder using PTL and explain how SUM and CARRY are generated.	L4	CO3	6 M
OR					
9	a)	Compare static CMOS and Domino logic.	L4	CO4	5 M
	b)	Explain the working of Domino logic with circuit diagram.	L3	CO4	5 M
UNIT-V					
10	a)	List and explain major steps involved in FPGA design flow.	L2	CO5	5 M
	b)	Explain how LUTs implement logic functions.	L3	CO5	5 M
OR					

11	a)	Introduce GaAs technology and its material properties.	L2	CO5	4 M
	b)	Explain the FinFET operation with advantages.	L3	CO5	6 M