PVP 23

Code: 23EC3601

III B.Tech - II Semester - Regular Examinations – APRIL 2026

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO
1.a)	Define output conductance (g_{ds}) in a MOS transistor.	L1	CO1
1.b)	What is channel length modulation?	L1	CO1
1.c)	How does scaling affect subthreshold leakage?	L2	CO1
1.d)	How does sheet resistance affect nMOS inverter?	L2	CO1
1.e)	A CS amplifier has gm = 2 mS and RD = 10 kΩ. Determine the voltage gain.	L3	CO2
1.f)	State the objective of preparing a stick diagram.	L1	CO3
1.g)	If VDD = 3.3 V and VT = 0.7 V, find output high level after one NMOS pass transistor.	L3	CO3
1.h)	Why is static power dissipation low in CMOS circuits?	L2	CO4
1.i)	What is the difference between simulation and synthesis in FPGA design?	L2	CO5

1.j)	Why is GaN suitable for high-power applications?	L2	CO5

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	With a neat circuit diagram, explain the operation of an nMOS inverter.	L2	CO1	5 M
	b)	Sketch and explain the Voltage Transfer Characteristics (VTC) of CMOS inverter.	L2	CO1	5 M
		OR			
3	a)	Interpret the drain current equation for MOS transistor in saturation.	L2	CO1	6 M
	b)	Differentiate between COMS and Bi-COMS technology.	L2	CO1	4 M
		UNIT-II			
4	a)	Describe the relation between resistivity and sheet resistance.	L2	CO1	6 M
	b)	Explain how sheet resistance applied for MOS circuits.	L2	CO1	4 M
		OR			
5	a)	Discuss the scaling factors for device parameters.	L2	CO1	7 M
	b)	Explain scaling limitation of current density.	L2	CO1	3 M

UNIT-III					
6	a)	Define a Common Drain amplifier with circuit diagram.	L1	CO2	3 M
	b)	Derive the voltage gain expression of Common Drain amplifier.	L4	CO2	7 M
OR					
7	a)	Explain lambda-based design rules.	L2	CO3	7 M
	b)	State advantages of λ-based methodology.	L2	CO3	3 M
UNIT-IV					
8	a)	Define Pass-Transistor Logic and explain its operating principle.	L1	CO3	4 M
	b)	Implement a Half Adder using PTL and explain how SUM and CARRY are generated.	L4	CO3	6 M
OR					
9	a)	Compare static CMOS and Domino logic.	L4	CO4	5 M
	b)	Explain the working of Domino logic with circuit diagram.	L3	CO4	5 M
UNIT-V					
10	a)	List and explain major steps involved in FPGA design flow.	L2	CO5	5 M
	b)	Explain how LUTs implement logic functions.	L3	CO5	5 M
OR					

11	a)	Introduce GaAs technology and its material properties.	L2	CO5	4 M
	b)	Explain the FinFET operation with advantages.	L3	CO5	6 M

PART-A

1. a) Definition (or) gds equations ----------2M

1.b) Definition----------2M

1.c) Equation ----------1M
affect ----------1M

1.d) Equation of Sheet Resistance----------1M
affect ----------1M

1.e) Formula----------1M
Answer----------1M

1.f) Definition or colours----------1M
Objective----------1M

1.g) Given data----------1M
Answer----------1M

1.h) Explanation----------2M

1.i) any one difference----------2M
1.j) Explanation----------2M

PART-B

2.a) Circuit diagram and Graph, truth table ----------3M
Explanation----------2M
2.b) Circuit diagram and Graph, truth table ----------3M
Explanation----------2M

3.a) Derivation of Current Equation ----------6M
3.b) Any four Comparisons----------4M

4.a) Sheet restance definition and Equation----------3M
Relation----------3M
4.b) Example MOS Circuit diagrams ----------2M
Calculations----------2M

5.a) Any 7 Scaling Factors----------7M
5.b) Explanation----------3M

6.a) Definition/introduction----------1M
Circuit diagram ----------2M
6.b) Derivation of Voltage gain and Equivalent circuit------7M

7.a) Definition ----------1M
Diagrams ----------6M
7.b) Any 3 Advantages----------3M

8.a) Definition and diagrams ----------4M
8.b) Half adder Truth Table and Equations----------3M
Circuit diagram using PTL----------3M

9.a) Any 4 Comparisons----------5M
9.b) Circuit diagram----------3M
Explanation----------2M

10.a) List and diagram----------3M
Explanation----------2M
10.b) Example Logic gate/Function Symbol----------2M
Implement of logic function using LUT----------3M

11.a) Introduction of GaAs ----------2M
Properties----------2M
11.b) Operation and Diagram of FinFET----------3M
Advantages----------3M

PART-A

1.a)

Ans)

- **The output conductance g_{ds} can be expressed as -**

$$g_{ds} = \frac{\delta I_{ds}}{\delta V_{gs}}$$

$$= \lambda \cdot I_{ds} = \left(\frac{1}{L}\right)^2$$

- **For the MOS device, strong dependence on the channel length demonstrated as -**

$$\lambda \propto \frac{1}{L} \quad \text{and}$$

$$I_{ds} \propto \frac{1}{L}$$

1.b)

Ans) Channel Length Modulation (CLM) is an effect in a MOSFET where the **effective channel length decreases slightly as the drain-to-source voltage (V_DS) increases**, even when the transistor is in saturation.

1.c)

Ans) Major concern in scaling devices is the effect on sub threshold current I sub

I sub is directly praportinal to exp (Vgs – Vt) q/KT.

When transistor is in off state the value of Vgs – Vt is negative and should be larger as possible to minimize I sub. As voltages are scaled down, ratio of Vgs-Vt to KT will reduce-so that threshold current increases.

1.d)

Ans)

Sheet resistance usually denoted as $R_s = \rho/t \quad \Omega/\square$

Rs=10k for n diffusion

Higher sheet resistance increase delay then Result **slower the inverter performance**

1.e)

Ans) given data gm=2ms and Rd=10K

Voltage gain = $-g_m R_d$

$= -2 \times 10^{-3} \times 10 \times 10^{3}$

$= -20$

1.f)

Ans) Stick diagram Convey the layer information through Color codes like

metal-Blue, n-diffussion-Green, p-diffusion-Yellow and Polysilicon-Red

the objective of preparing a stick diagram in VLSI design is to give a **simple, easy to design and visual representation of a circuit layout** without exact dimensions.

1.g)

Ans) Given data Vdd= 3.3V and VT=0.7V

Output of one NMOS transistor =3.3-0.7=2.6V

1.h)

Ans) Static power dissipation in **CMOS circuits** is very low mainly because of CMOS gate is a **stable**

logic state:

- One transistor is **ON**
- The other is **OFF**

This means there is **no direct path from power supply (V_DD) to ground**.

So, **Istatic≈0⇒Pstatic=V×I≈0**

1.i)

Ans)

The HDL code is simulated using **simulation** tools to verify the functionality and behavior of the design

During **synthesis**, the HDL code is translated into a gate-level netlist, which is a representation of the design using logic gates and their interconnections.

1.j)

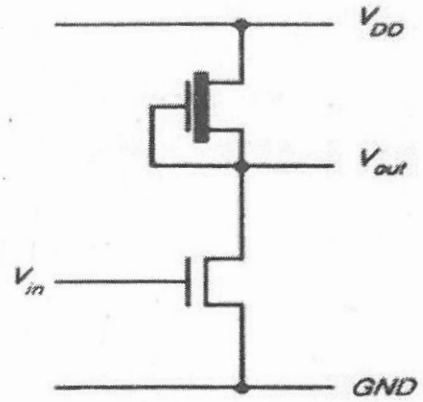
Ans) **Gallium Nitride (GaN)** is especially well-suited for high-power applications because its material Properties allow devices to handle **higher voltages, Reduce leakage currents, and temperatures** more efficiently than traditional silicon

PART-B

2.a

Ans)

The nMOS INVERTER



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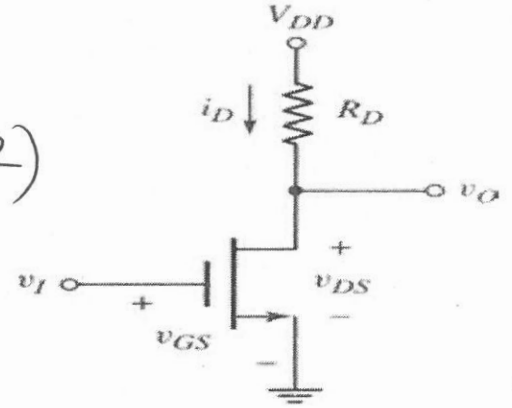


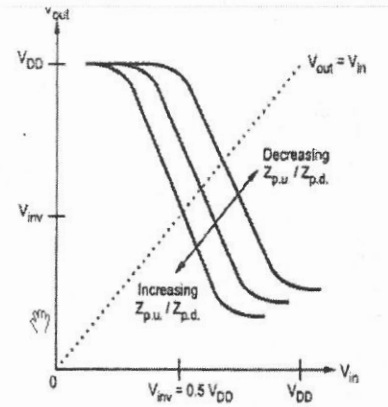
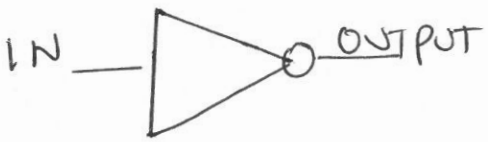


Fig. 2.32 nMOS inverter transfer characteristic



IN	OUTPUT
0	1
1	0

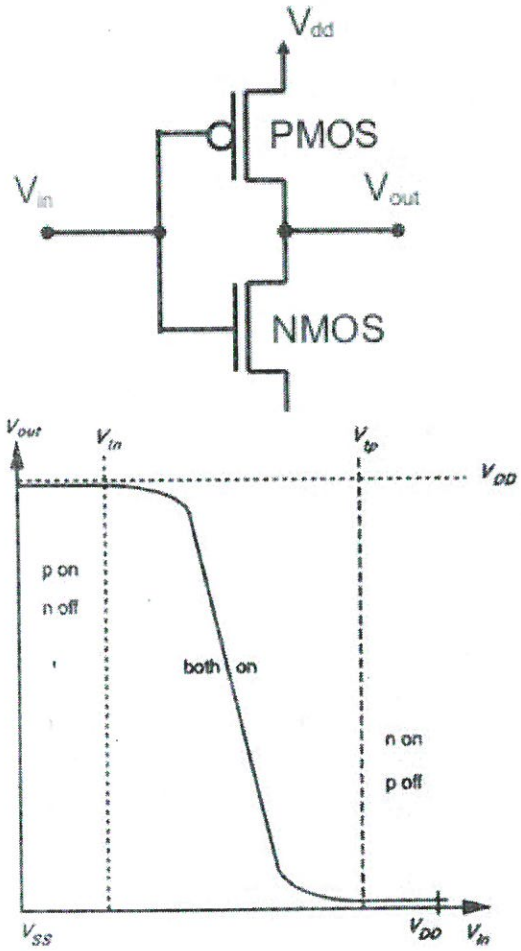
1. Vin =0V, Pull up transistor (or) depletion mode transistoror is ON, NMOS Transistor or enhancement mode Transistor is OFF and the entire power supply flows towards output terminal, so that output is V_{DD}
   - **V_{out}= V_{DD}= Logic 1**
2. Vin =0V, PMOS Transistor ON, NMOS Transistor OFF, the entire power supply flows towards output terminal, so that output is oV

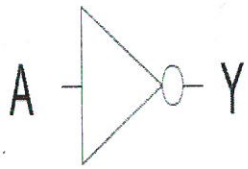
   V_{out}= oV= Logic 0

2.b)

Ans) CMOS Inverter: Complementary metal oxidesemiconductor

As shown in the diagram below the CMOS transistor is designed using p-MOS and n-MOS transistors.





IN A	OUT Y
0	1
1	0

Fig: Voltage transfer function

1. Vin =0V, PMOS Transistor (or) Pull up transistor is ON, NMOS Transistor or Pull down Transistor is OFF and the entire power supply flows towards output terminal, so that output is **V_{DD}**

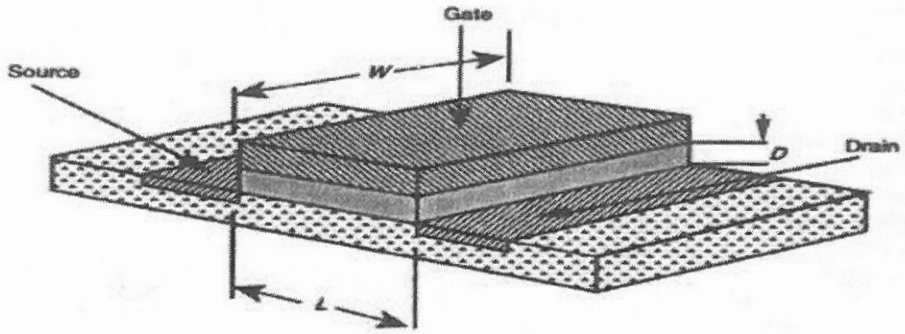
   V_{out}= V_{DD}= Logic 1

2. Vin =0V, PMOS Transistor ON, NMOS Transistor OFF, the entaier power supply flows towards output terminal,sothat output is oV

   V_{out}= oV= Logic 0

3.a)

Ans)



2.1.2 Saturated Region

- The device enters into saturation when $V_{ds} = V_{gs} - V_t$, because at this point the IR drop in the channel equals the effective gate to channel voltage. The current through the channel remains fairly constant for any further increase in V_{ds}.

$$I_{ds} = K\frac{W}{L}\frac{(V_{gs} - V_t)^2}{2} \quad \text{...(2.17)}$$

$$I_{ds} = \frac{\beta}{2}\cdot(V_{gs} - V_t)^2 \quad \text{...(2.18)}$$

$$I_{ds} = \frac{\mu C_{g-ch}}{2L^2}(V_{gs} - V_t)^2 \quad \text{...(2.19)}$$

$$\boxed{I_{ds} = C_o \cdot \mu \cdot \frac{W}{2L} \cdot (V_{gs} - V_t)^2} \quad \text{... (2.20)}$$

3.b)

Ans)

CMOS	Bi-CMOS
1.Complementary metal oxide semiconductor	Combination of Both CMOS and BJT
2.Low Power Consumption	High Power Consumption compered to CMOS
3.Low Speed compared to Bi-CMOS	High Speed
4.Lower current drive	High current drive
5.Low Cost	High Cost
6.Low gm	High gm
7.Simpler fabrication process	More complex (needs both CMOS and bipolar fabrication steps)
8.High Density	Less Density
9.It is used digital ICs	It is used High-speed & analog circuits

4.a)

Ans) The sheet resistance is a measure of resistance of thin films that have a uniform thickness. It is commonly used to characterize materials made by semiconductor doping, metal deposition, resistive paste printing, and glass coating.

Example of these processes are: doped semiconductor regions (eg: silicon or polysilicon) and resistance

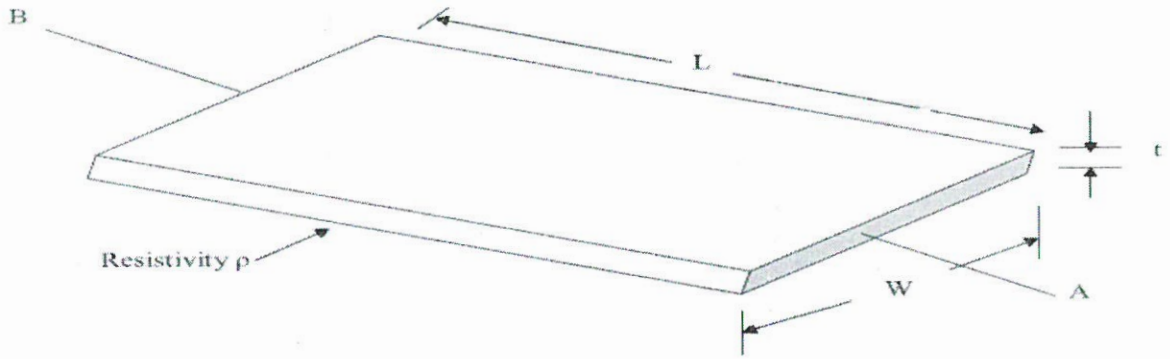
Consider a uniform slab of conducting material of resistivity ρ, of width W, thickness t, and length between faces L as shown below:

$$R_{AB} = \frac{\rho L}{tW} \quad \text{ohm}$$

Where A = cross section area.

Thus $R_{AB} = \frac{\rho L}{tW}$ ohm.

When L = W, i.e. a square resistive material, then



$$R_{AB} = \frac{\rho}{t} = R_s$$

Where R_s =ohm per square or sheet resistance.

Thus $R_s = \frac{\rho}{t}$ ohm per square.

It is completely independent of the area of the square.

4.b)

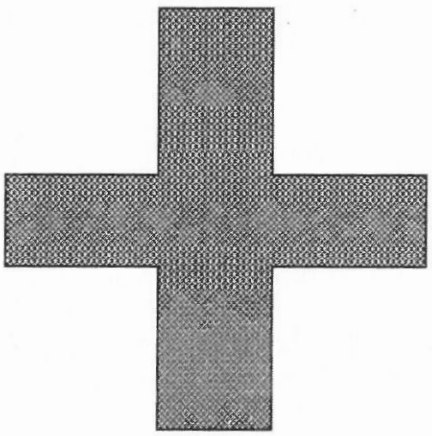
Where R_s =ohm per square or sheet resistance.

Ans)

Thus $R_s = \frac{\rho}{t}$ ohm per square.

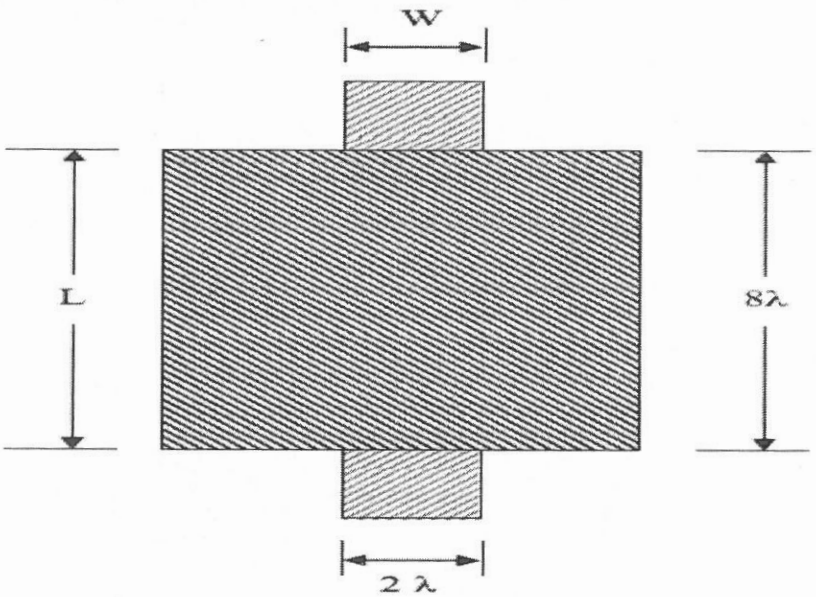
Sheet resistance concept applied to MOS circuits

The simple n-type pass transistor has a channel length L = 2λ and a channel width W = 2 λ. The channel is square



$$R = \text{square X } R_s \frac{Ohm}{square} = R_s = 10^4 \text{ ohm.}$$

The length to width ratio, denoted by Z is 1:1 in this case. Consider one more structure as in diagram below.

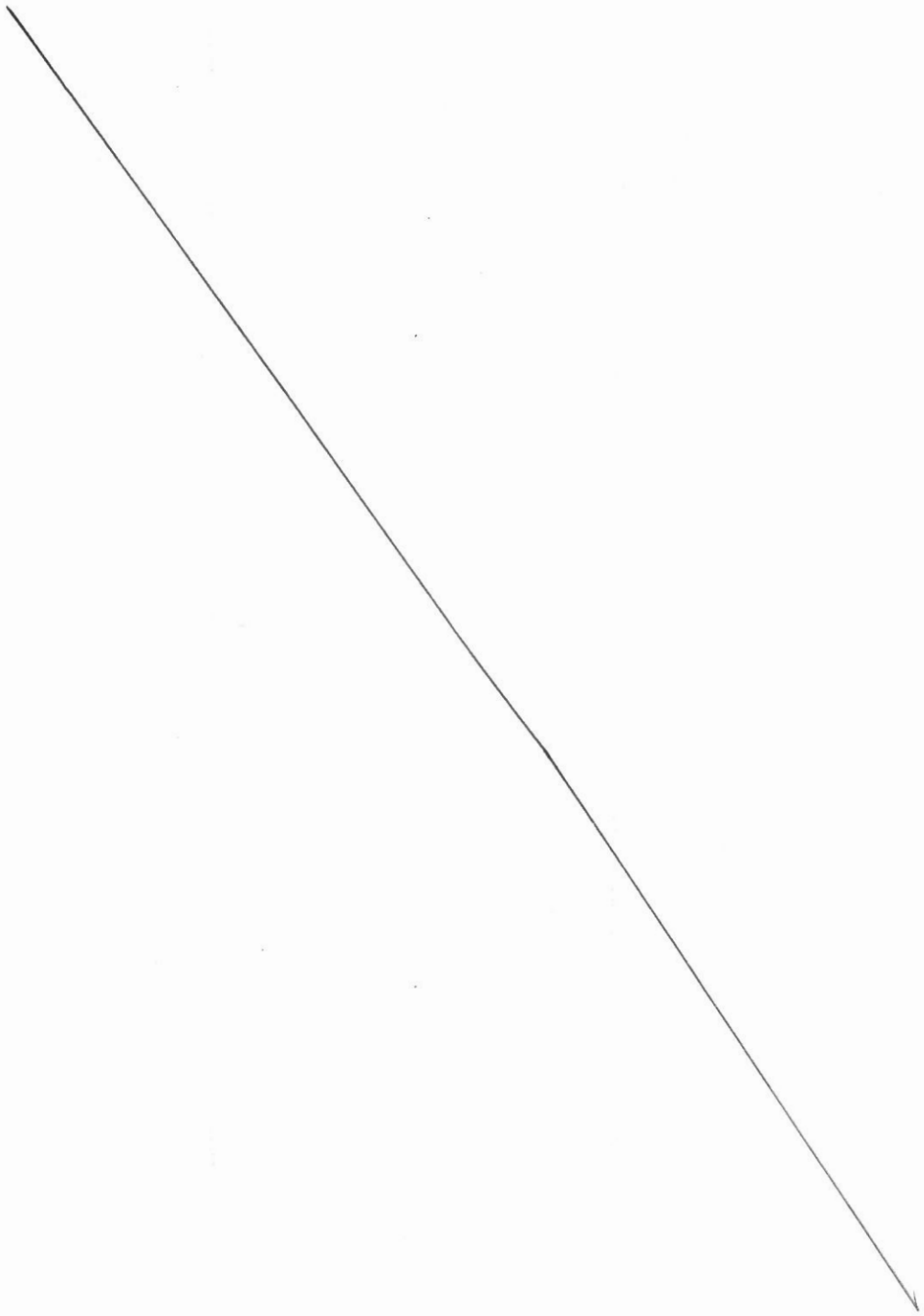


$L = 8\ \lambda$ and $W = 2\ \lambda$

$Z = \frac{L}{W} = 4$

Channel resistance $R = Z R_s = 4 \times 10^4$ Ohm.

This channel can be taken as four 2 λ X 2 λ squares in series.



5(a) 1) Scale Area A_g

$$A_g = L \times w$$

$$L = 1/\alpha$$

$$w = 1/\alpha$$

$$A_g = \frac{1}{\alpha} \times \frac{1}{\alpha}$$

$$A_g = 1/\alpha^2$$

A_g scaled by $1/\alpha^2$

2) Scale capacitance per unit area C_0 ($\overline{C_1}$) C_{ox}

$$C_{ox} = \frac{\varepsilon_{ox}}{D}$$

where D - is oxide thickness

$$D = \frac{1}{\beta}$$

$$\varepsilon_{ox} = 1$$

$$C_{ox} = \frac{1}{1/\beta} = \beta$$

~~$C_{ox} = C_0 = 1$~~

$$\boxed{C_{ox} = C_0 = \beta}$$

3) Scale capacitence C_g

$$C_g = C_0 \times L \times w$$

$$= \beta \times \frac{1}{\alpha} \times \frac{1}{\alpha}$$

$$\boxed{C_g = \frac{\beta}{\alpha^2}}$$

C_g scaled by β/α^2

4) parasitic capacitance C_x

$$C_x = \frac{A_x}{d} = \frac{\frac{1}{\alpha^2}}{1/\alpha}$$

$$\boxed{C_x = 1/\alpha}$$

5) Current Density in channel $\overline{Q_{on}}$

$$\overline{Q_{ON}} = C_0 \times V_{gs}$$

$$\overline{Q_{ON}} = C_0 \times V_{gs} \quad (V_{gs} = \frac{1}{\beta})$$

$$\overline{Q_{on}} = \beta \times \frac{1}{\beta}$$

$$\boxed{\overline{Q_{on}} = 1}$$

Thus $\overline{Q_{on}}$ scaled by 1

6) Channel Resistance R_{on}

$$R_{on} = \frac{L}{w} \times \frac{1}{\overline{Q_{on}} \times \mu}$$

where μ = channel carrier mobility and assumed constant

$$R_{ON} = \frac{\frac{1}{\alpha}}{1/\alpha} \times \frac{1}{1 \times 1}$$

$$\boxed{R_{ON} = 1}$$

R_{ON} is scaled by 1

7) Scale Delay T_d

$$T_d = R_{ON} \times C_g$$

$$= 1 \times \beta/\alpha^2$$

$$\boxed{T_d = \frac{\beta}{\alpha^2}}$$

8) Maximum operating freq f_0

$$f_0 = \frac{w}{L} \times \frac{\mu C_0 V_{DD}}{C_g} \quad (\because V_{DD} = \frac{1}{\beta})$$

$$= \frac{1}{\frac{1}{\alpha}} \times \frac{1 \times \beta \times \frac{1}{\beta}}{\beta/\alpha^2}$$

$$\boxed{f_0 = \frac{\alpha^2}{\beta}}$$

f_0 scaled by α^2/β

9) Saturation Current I_{dss}

$$I_{dss} = \frac{C_{ox}\mu}{2} \times \frac{W}{L} \times (V_{gs} - V_t)^2$$

Both V_{gs} and V_t are scaled by $1/\beta$

$$I_{dss} = \frac{\beta \cdot 1}{2} \times \frac{1/\alpha}{1/\alpha} \times \frac{1}{\beta^2} = \frac{\beta}{2\beta^2} = \frac{1}{2\beta}$$

$$\boxed{I_{dss} = \frac{1}{\beta}}$$ $\therefore$ I_{dss} Scaled by $\frac{1}{\beta}$

10) Current Density J

$$J = \frac{I_{dss}}{A} = \frac{\frac{1}{\beta}}{1/\alpha^2}$$

$$\boxed{J = \frac{\alpha^2}{\beta}}$$ $\therefore$ current Density J is Scaled by α^2/β

11) Switching Energy per Gate E_g

$$E_g = \frac{1}{2} C_g V_{DD}^2 \qquad \left(V_{DD} = \frac{1}{\beta}\right)$$

$$= \frac{1}{2} \frac{\beta}{\alpha^2} \frac{1}{\beta^2}$$

$$= \frac{1}{2\alpha^2\beta}$$

$$\boxed{E_g \sim \frac{1}{\alpha^2\beta}}$$ E_g Scaled by $\frac{1}{\alpha^2\beta}$

12) Power dissipation per gate P_g

$$P_g = P_{gs} + P_{gd}$$

P_g Comprises of two Components: Static power Component P_{gs} and dynamic power Component P_{gd}

12) Static power compact is given by

$$P_{gs} = \frac{V_{DD}^2}{R_{ON}} = \frac{1}{\frac{\beta^2}{1}}$$

$$P_{gs} = \frac{1}{\beta^2} \quad (\because V_{DD} = \frac{1}{\beta})$$

Dynamic power component is given by

$$P_{gd} = E_g f_0$$

$$= \frac{1}{\alpha^2 \beta} \times \frac{\alpha^2}{\beta}$$

$$P_{gd} = \frac{1}{\beta^2}$$

$$P_g = P_{gs} + P_{gd} = \frac{1}{\beta^2} + \frac{1}{\beta^2} = \frac{2}{\beta^2}$$

$$= \frac{\cancel{2}}{\cancel{2}}$$

$$\boxed{P_g = \frac{1}{\beta^2}}$$

13) Power dissipation per unit area $P_a = \frac{P_g}{A_g}$

$$= \frac{\frac{1}{\beta^2}}{\frac{1}{\alpha^2}} = \frac{\alpha^2}{\beta^2}$$

$$\boxed{P_a = \frac{\alpha^2}{\beta^2}}$$

14) Power - Speed product (P

$$P_T = P_g \times T_d$$

$$= \frac{1}{\beta^2} \times \beta/\alpha^2$$

$$\boxed{P_T = \frac{1}{\alpha^2 \beta}}$$

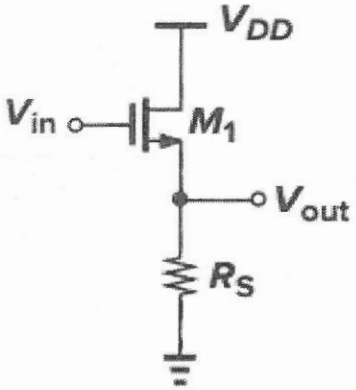
5.b)

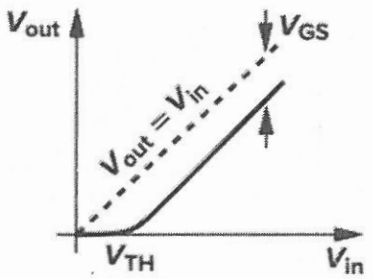
Ans) Scaling Limitation due to current density:

- High purity aluminium the most attractive material for forming interconnections in VLSI chips
- Scaling down of dimensions also increases the current density in interconnects if constant field scaling is applied.
- When the current density in aluminium approaches 106Amps/cm square(10amps/micrometer square) the interconnects are burned off owing to material migration.
- So allowable current densities are set well below this limit and figures of J=1 to 2 mA/micrometer square are commonly used

6.a)

Ans) a **common-drain** amplifier, also known as a **source follower** can operate as a **voltage buffer**. In this circuit (NMOS) the gate terminal of the transistor serves as the signal input, the source is the output, and the drain is *common* to both (input and output), hence its name. Because of its low dependence on the load resistor on the voltage gain, it can be used to drive low resistance loads, such as a speaker. The analogous bipolar junction transistor circuit is the common-collector amplifier. This circuit is also commonly called a "stabilizer".



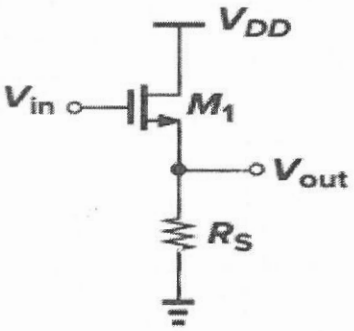


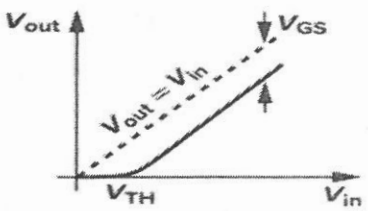
(c)

1 (c) its input-output characteristic.

6.b)

Ans)





(c)

1 (c) its input-output characteristic.

that for $V_{in} < V_{TH}$, M_1 is off and $V_{out} = 0$. As V_{in} exceeds V_{TH}, M_1 turns on in saturation (why?) and I_{D1} flows through R_S [Fig. 3.34(c)]. As V_{in} increases further, V_{out} follows the input with a difference (level shift) equal to V_{GS}. We can express the input-output characteristic as

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out} \tag{3.82}$$

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out} \tag{3.82}$$

where channel-length modulation is neglected. Let us calculate the small-signal gain of the circuit by differentiating both sides of (3.82) with respect to V_{in}:

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}2(V_{in} - V_{TH} - V_{out})\left(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}\right)R_S = \frac{\partial V_{out}}{\partial V_{in}} \tag{3.83}$$

Since $\partial V_{TH}/\partial V_{in} = (\partial V_{TH}/\partial V_{SB})(\partial V_{SB}/\partial V_{in}) = \eta \partial V_{out}/\partial V_{in}$,

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox}\dfrac{W}{L}(V_{in} - V_{TH} - V_{out})R_S}{1 + \mu_n C_{ox}\dfrac{W}{L}(V_{in} - V_{TH} - V_{out})R_S(1+\eta)} \tag{3.84}$$

Also, note that

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out}) \tag{3.85}$$

Consequently,

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S}$$

(OR)

The same result is more easily obtained with the aid of a small-signal equivalent circuit. From Fig. 3.35, we have $V_{in} - V_1 = V_{out}$, $V_{bs} = -V_{out}$, and $g_m V_1 - g_{mb} V_{out} = V_{out}/R_S$. Thus, $V_{out}/V_{in} = g_m R_S/[1 + (g_m + g_{mb})R_S]$.

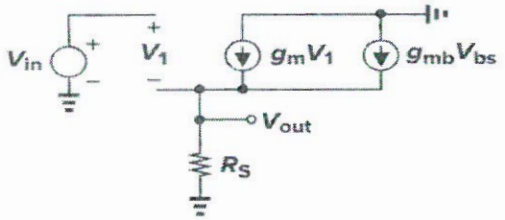


Figure 3.35 Small-signal equivalent circuit of source follower.

7.a)

Ans) λ Based Design Rules: Developed by Mead and Conway popularized λ Based Design Rules based on single parameter.All device dimensions are expresses in terms of a scalable parameter λ.

λ = L/2; L = The minimum feature size of transistor

L = 2 λ

These rules support proportional scaling.

They should be applied carefully in sub-micron CMOS process

In MOS, the minimum feature size of Tr is:

- (L/W)n = 1/1 = 2 λ/2 λ Active area = L*W = 4 λ^2

In CMOS, the minimum feature size of Tr is:

- (L/W)n = 1/1.5 = 2 λ/3 λ Active area = L*W = 6 λ^2

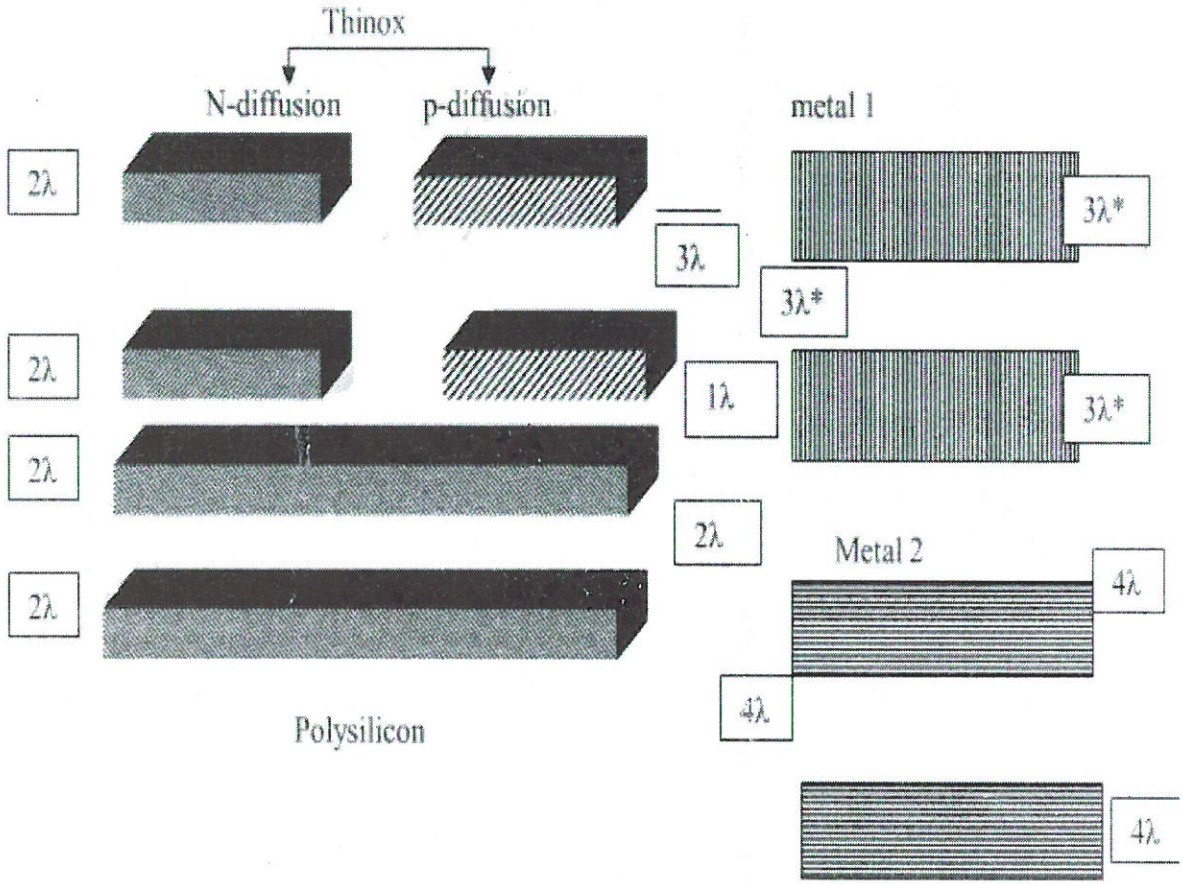
LAMBDA BSED RULES

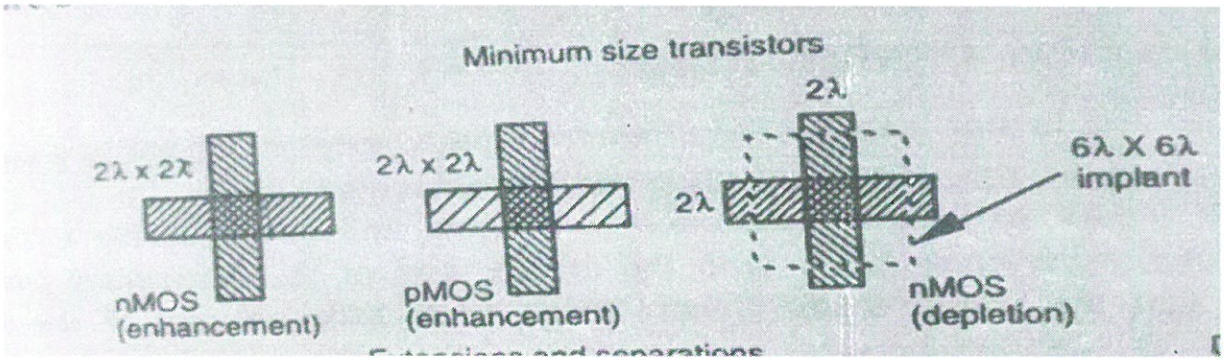
MINIMUM WIDTH AND SPACING RULES

LAYER	TYPE OF RULE	VALUE
POLY	Minimum Width Minimum Spacing	2λ 2λ
N/P DIFFUSION	Minimum Width Minimum Spacing	3λ 3λ
N-WELL	Minimum Width Minimum Spacing	3λ 3λ
P-WELL	Minimum Width Minimum Spacing	3λ 3λ
METAL1	Minimum Width Minimum Spacing	3λ 3λ

Minimum width specified)

minimum separation (where





y: Polysilicon n-diffusion p-diffusion Transistor channel (polysilicon over thinox)

FIGURE 3.7 Transistor design rules (nMOS, pMOS and CMOS).

7.b)

Ans) Advantages of Lamba based Design Rules:

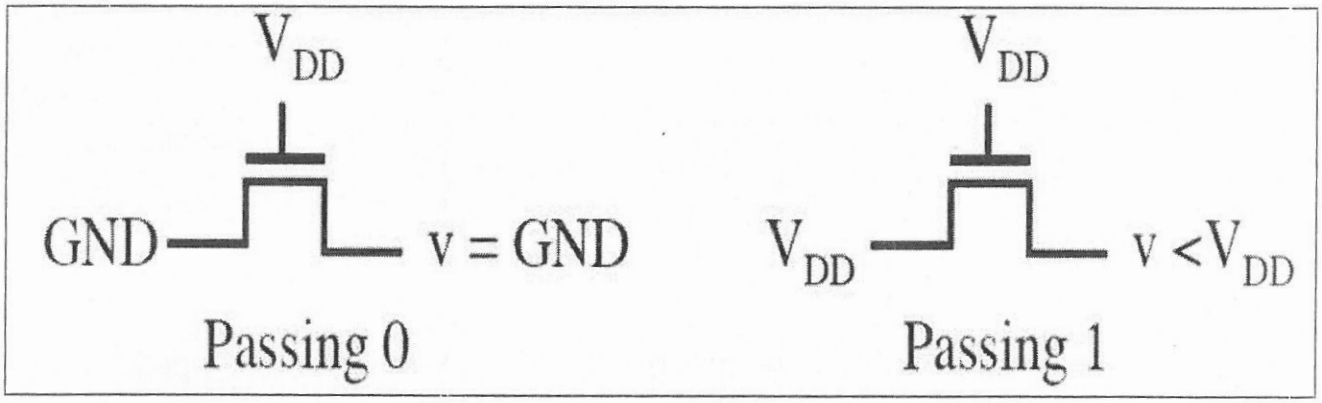
- These rules support proportional scaling.
- Simple Design and Easy to Understand
- They should be applied carefully in sub-micron CMOS process
- Design rules are a set of geometrical specifications that dictate the design of the layout masks
- A design rule set provides numerical values
  - For minimum dimensions
  - For minimum line spacings
- Design rules must be followed to insure functional structures on the fabricated chip.
- Design rules change with technological advances

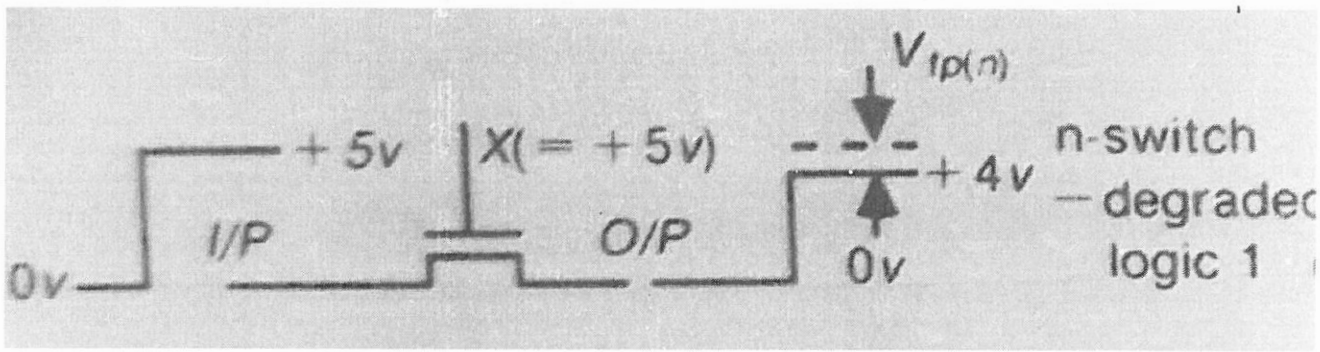
8.a)

Ans)

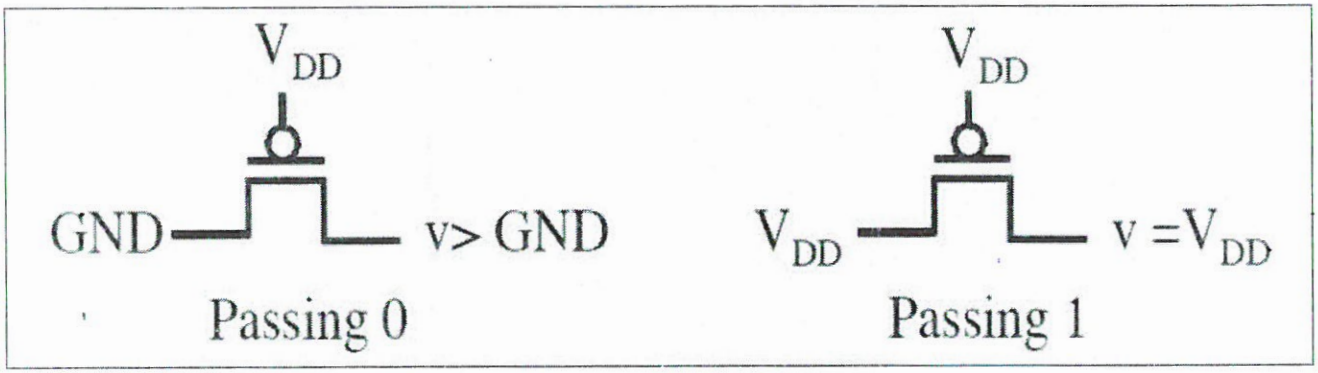
Pass Transistor Logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.

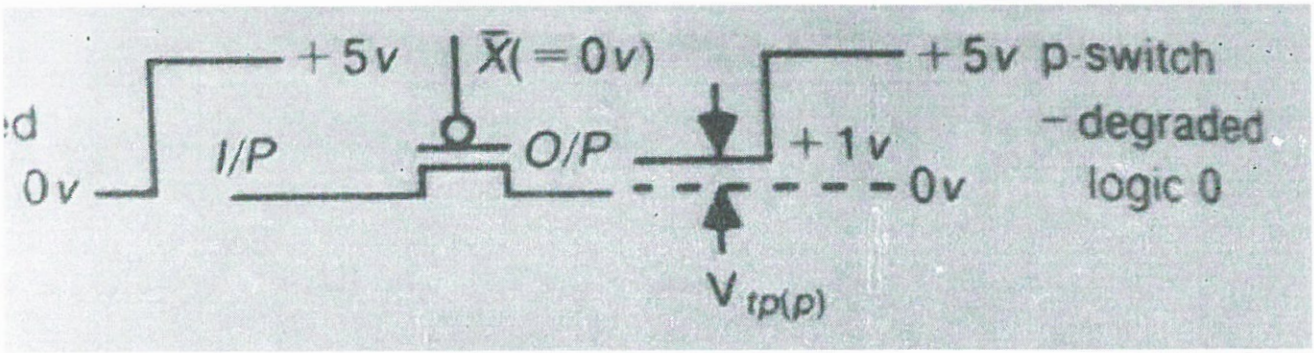
N-Channel MOS Transistors pass a 0 better than a 1



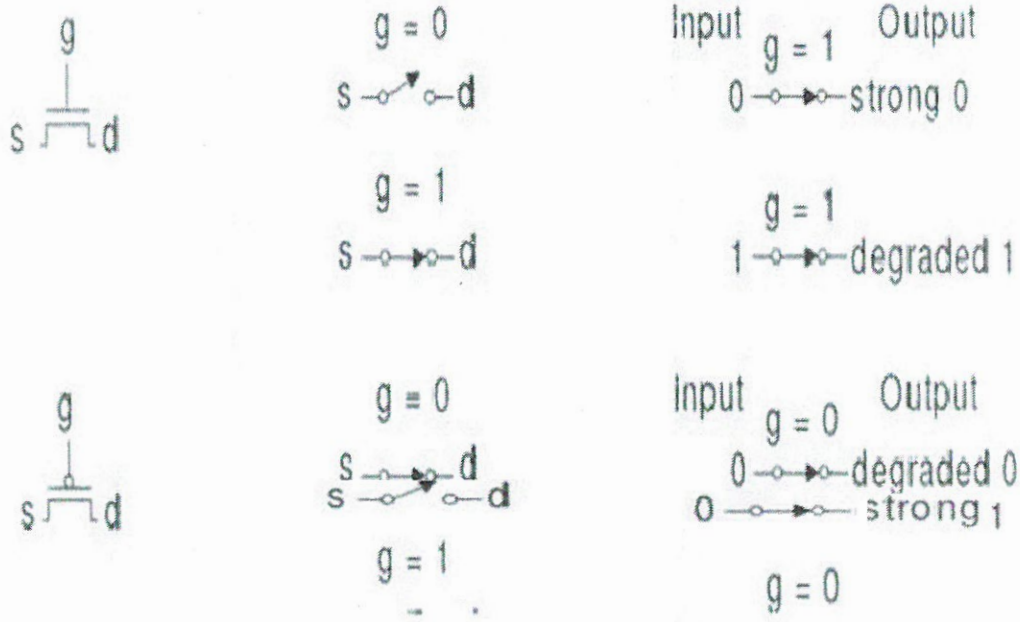


- P-Channel MOS Transistors pass a 1 better than a 0





- Switch logic:pass transistor



10

8.b)

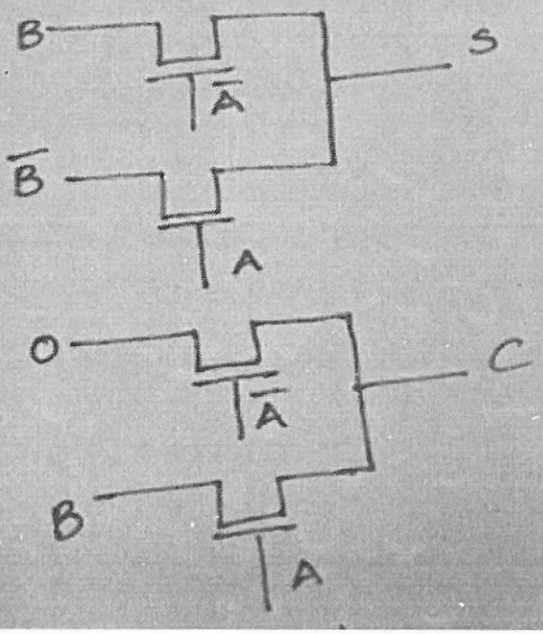
Ans) Half Adder Using Pass Transistor Logic

Truth table

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = \bar{A}B + A\bar{B} = A \oplus B$

$C = A \cdot B$



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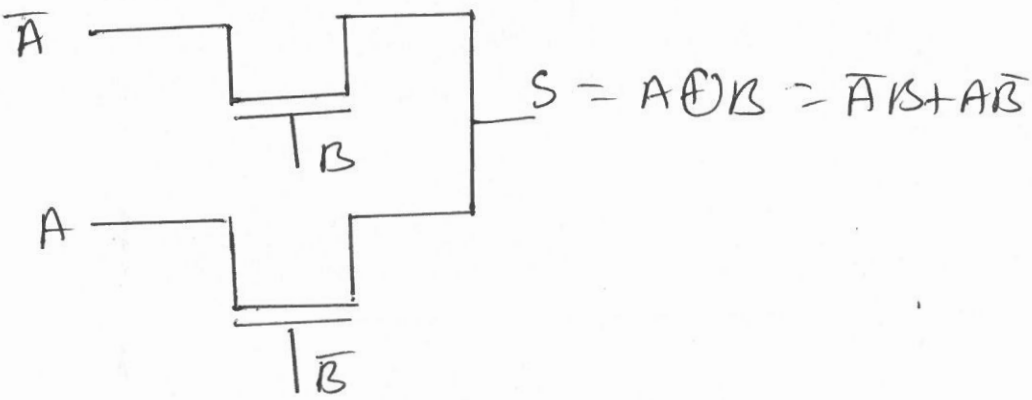

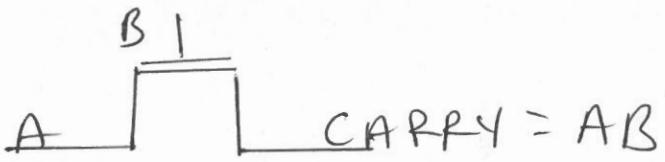

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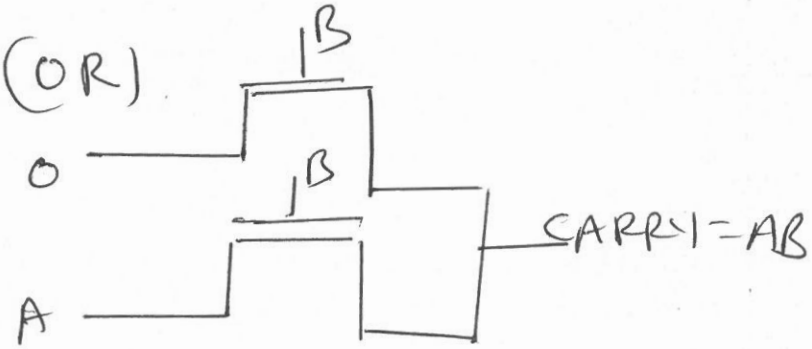
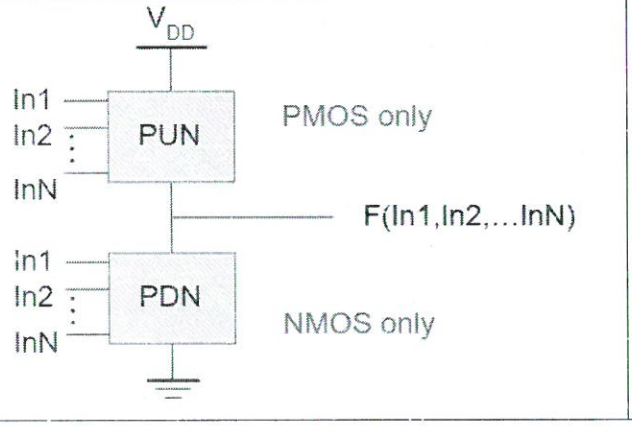
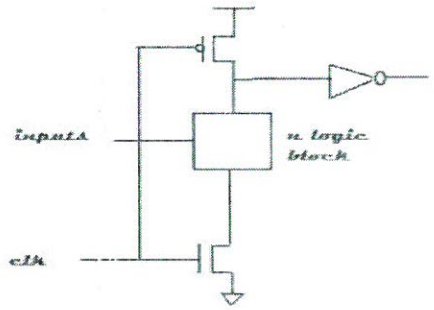


9.a)

Ans)

STATIC	DOMINO
1.It uses both Pull Up and Pull Down Networks	It uses only Pull Down Network
2.Not required Clock	required Clock
3.Moderate Speed	High Speed
4.Low Power Consumption	High Power Consumption
5.Output depends directly on inputs	Two phases: Precharge and Evalution
6.Simple Design	More Complex
7.High Noise Immunity	Low Noise Immunity
8.Lage area (PMOS+NMOS)	Small area (NMOS only)
9.High Reliability	Lower Reliability
	

9.b)Ans) **Domino Logic**

A domino logic consist of an n-type dynamic logic block followed by a static inverter.

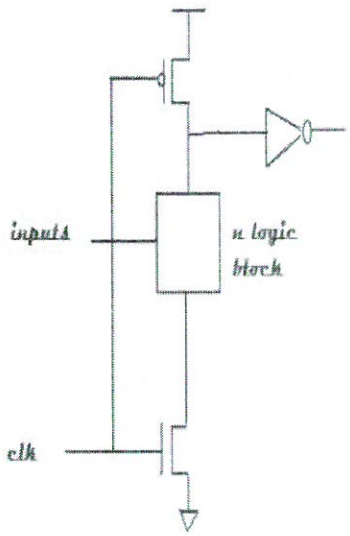
During precharge - the output is charged to VDD, so the output of the inverter becomes zero.

During evaluation mode – the gate conditionally discharges and the ouput of inverter becomes one.

- In this we are able to cascade logic blocks with the help of a single clock. The precharge and the evaluate phases retained as they were.

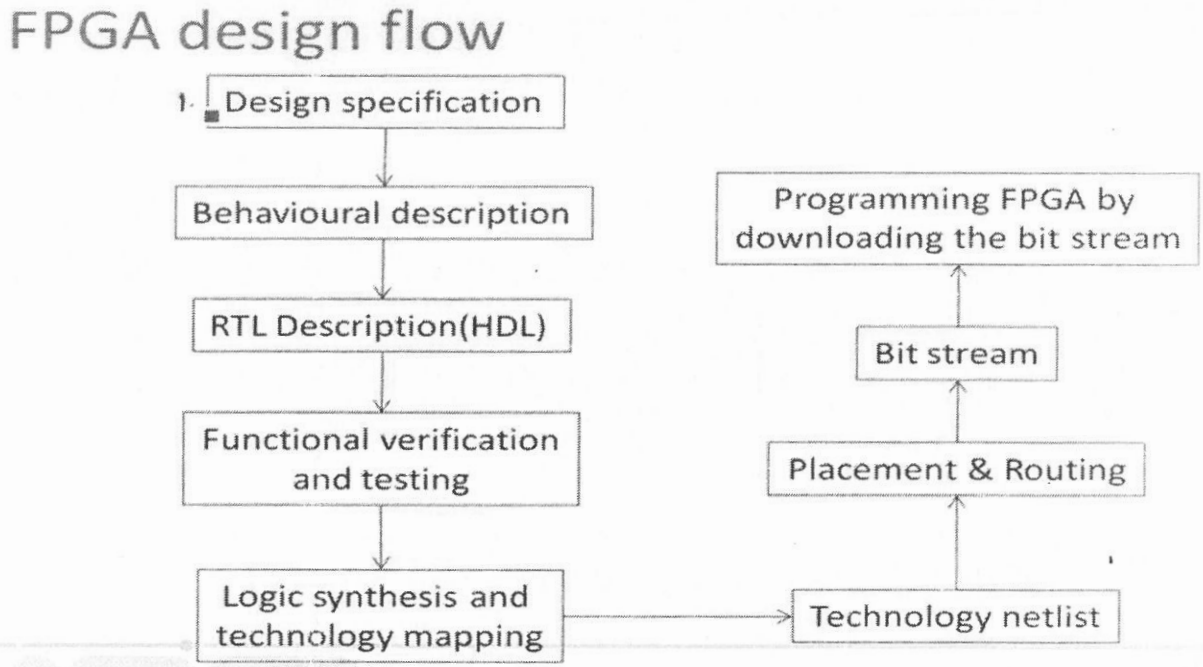
- The change required is to add a buffer at the end of each stage.

- This logic works in the following manner. When the clk=0,ie during the precharge stage the output of the dynamic logic is high and the output of the buffer is low.
- When the gate is evaluated in the next phase, the output conditionally goes low and the output of the buffer goes high.



10.a)

Ans)



1.Design Spesication

2.Behavioral Desrption

3. Register Transfer Level Description

4. Functional Verification and Testing or Design Simulation

5. **Logic Synthesis and technology Mapping**

6. Programming/Configuration

7. Place and Route

8. **Bitstream Generation**

The FPGA design flow refers to the sequential steps involved in developing a design for implementation on an FPGA device. The design flow typically consists of the following main stages:

1.Design Spesication

- This is the initial stage where the design is specified using a hardware description language (HDL) such as Verilog or VHDL.
- The design can also be captured using schematic entry tools or high-level synthesis tools, which automatically generate HDL code from C/C++ or other high-level languages.

a. Behavioural description :- we are writing the behaviour of H/w in a programming language.

↳ VHDL (Very high speed IC H/w description language)
↳ Verilog HDL

2-ip AND gate :- a, b — in
y — out
y <= a and b;

a. Behavioural description :- we are writing the behaviour of H/w in a programming language.

↳ VHDL (Very High Speed IC H/w description language)
↳ Verilog HDL

2-i/p AND gate :- a, b — in
y — out
y <= a and b;

3.Register Transfer Level Description: Register Transfer level means specifying how the data flows between registers and how the design processes the data. The behavioral description is manually converted to an RTL description in an HDL

4.Functional Verification and Testing or Design Simulation

- The HDL code is simulated using simulation tools to verify the functionality and behavior of the design.
- Simulation is an essential step to catch and fix any design errors or bugs before synthesis

Here errors are verified. Once it is correct next step is to verify the i/p o/p.

y <= a and b;

a = 0
b = 1

y <= 0 and 1;

y <= 0 ✓

5.Logic Synthesis and technology Mapping:

During synthesis, the HDL code is translated into a gate-level netlist, which is a representation of the design using logic gates and their interconnections.

The synthesis tool maps the HDL constructs to the available resources on the target FPGA device, such as look-up tables (LUTs), registers, and dedicated blocks like memories or DSP slices.the following technology mapping

FPGA → Artix, Altera, Virtex,

6.Programming/Configuration

The generated bitstream is loaded onto the FPGA device, configuring it to implement the desired design.This can be done using various programming interfaces and methods, such as JTAG, SPI, or dedicated configuration ports

7.Place and Route

The place and route stage involves physically mapping the synthesized netlist onto the FPGA device.

The placement step determines the physical location of the logic elements on the FPGA fabric.

The routing step establishes the interconnections between the logic elements using the programmable routing resources of the FPGA.

8.Bitstream Generation

The final step is the generation of a bitstream, which is a binary file containing the configuration data for the FPGA device.

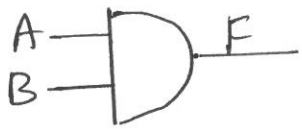
The bitstream encodes the logic functions, interconnections, and settings for the various components within the FPGA.

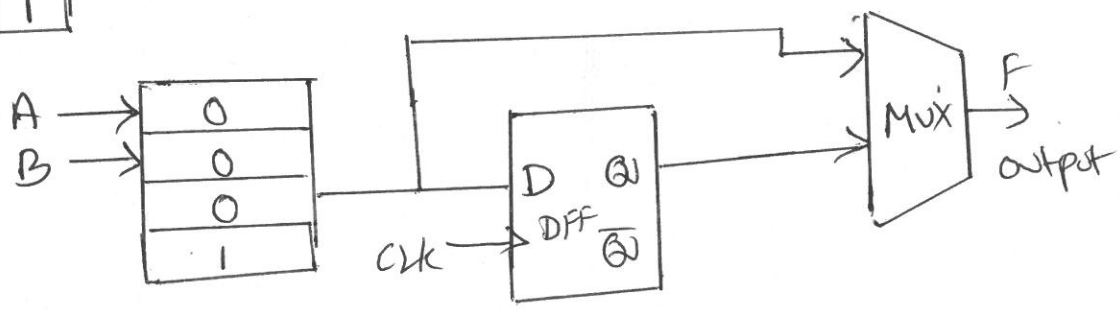
10 b) Implementation of LUT explain with example

Consider 2 Input AND Gate

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

$F = AB$





2-Input LUT has 4 Memory locations ($2^2=4$)

Each location Stores 1 output bit

Address (AB)	Stored Value
0 0	0
0 1	0
1 0	0
1 1	1

So, the LUT Content is 0, 0, 0, 1

NOTE: Consider Any logic Gate (or) Logic Function

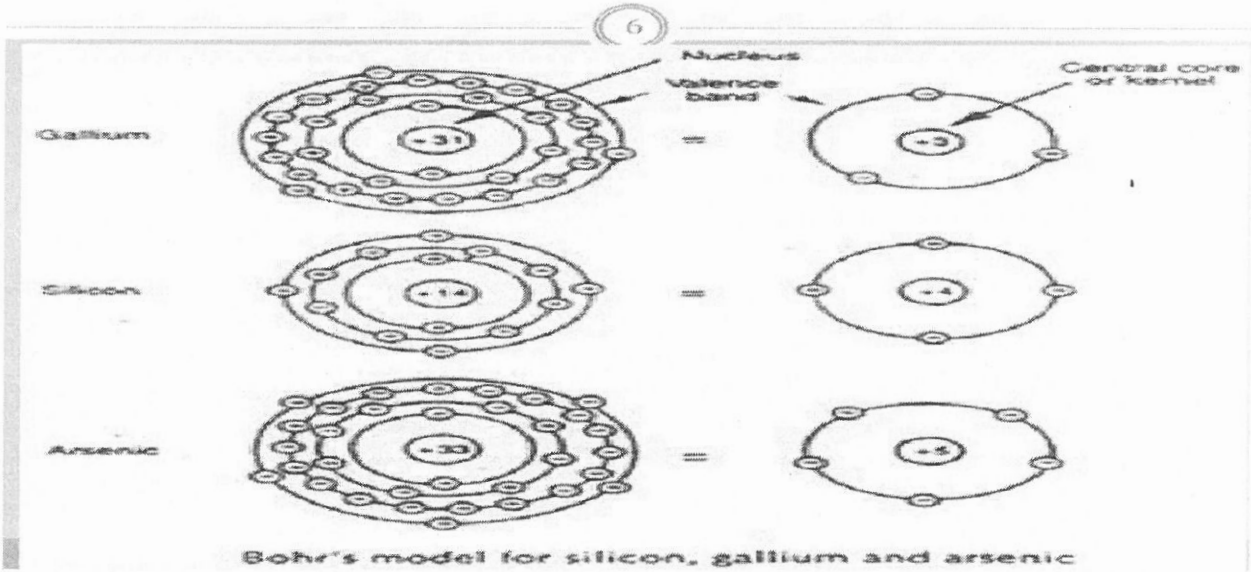
13

11.a)

Ans) Introduction of Gallium Arsenide (GaAs) technology

Gallium Arsenide (GaAs) VLSI technology offers superior high-speed, low-power, and radiation-hardened performance compared to silicon, utilizing high electron mobility for applications like aerospace, telecom, and high-performance computing. It uses semi-insulating substrates for low parasitic capacitance and uses specialized logic families like DCFL (Direct-Coupled FET Logic) and HEMTs (High-Electron-Mobility Transistors) for very high speed

GaAs crystal structure...



The higher electron mobility for GaAs shows promise for high speed devices and circuits. The direct gap allows for emission of photons in LEDs and LASER devices.

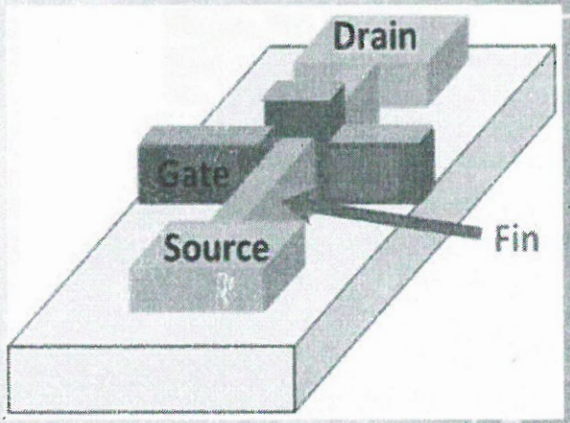
	GaAs
Minority Carrier Lifetime	1E-8
Electron Mobility	8000
Hole Mobility (cm2/Vs)	400
Energy Gap (eV)	1.43 (direct)
Vapor Pressure	1@1050C

11.b)

Ans)

INTRODUCTION

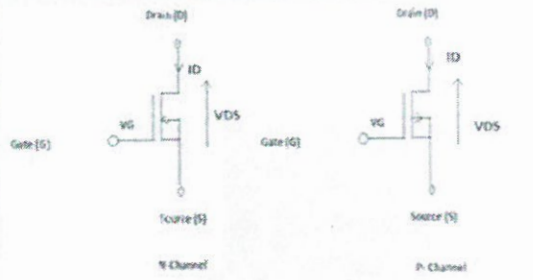
- The term "FINFET" describes a non-planar, double gate transistor built on an SOI substrate, based on the single gate transistor design.



- The important characteristics of FINFET is that the conducting channel is wrapped by a thin Si "fin", which forms the body of the device.
- The thickness of the fin determines the effective channel length of the device.

WORKING OF A FINFET

- The working principle of a FinFet is similar to that of a conventional MOSFET.
- The MOSFET can function in two modes for both p-channel and n-channel MOSFETs: enhancement mode and depletion mode
- The channel shows maximum conductance when there is no voltage on the gate terminal.
- As the voltage changes to positive or negative, the conductivity of the channel reduces.



- In enhancement mode of MOSFET, when there is no voltage on the gate terminal, it does not conduct.
- Unlike the depletion mode, in enhancement mode, the device conducts better when there is more voltage on the gate terminal.

Advantages of FinFET:

- Higher technological maturity than planar DG.
- Suppressed Short Channel Effect(SCE)
- Better in driving current
- More compact
- Low cost