PVP 23

Code: 23EE3502

III B.Tech - I Semester - Regular Examinations - NOVEMBER 2025

DIGITAL CIRCUITS
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

BL – Blooms Level CO – Course Outcome

PART – A

		BL	CO
1.a)	Show the use of don't care terms in K-map simplification.	L3	CO2
1.b)	Simplify F(A,B)=A'B+AB using Boolean theorems.	L3	CO1
1.c)	Distinguish between ROM and RAM.	L2	CO3
1.d)	Show two advantages of PLA over PAL.	L3	CO3
1.e)	State the function of a universal shift register.	L3	CO3
1.f)	Write the logic expression to convert the JK flip-flop to a T flip-flop.	L2	CO1
1.g)	Define state reduction.	L1	CO4
1.h)	Classify two methods of state assignment.	L2	CO4
1.i)	List any two features of TTL logic family.	L1	CO4
1.j)	Define power dissipation in digital ICs.	L1	CO1

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	Simplify the Boolean function, (A,B,C,D) = Σ(0,1,2,5,8,9,10,14) using K-map and draw the logic circuit.	L3	CO2	5 M
	b)	Explain that the universal logic gates are commutative but not associative.	L2	CO1	5 M
		OR			
3	a)	Draw the logic circuits using AND, OR and NOT elements to represent the following expressions: i. $A\bar{B} + \bar{A}\,B$ ii. $A + B[C + D(B + \bar{C})]$	L2	CO1	5 M
	b)	Simplify the following expression using Quine McClausky method and verify using K-map. F(A,B,C,D) = Σ(0,1,2,3,4,6,8,10,12,14)	L3	CO2	5 M
		UNIT-II			
4	a)	Distinguish between a decoder and a demultiplexer.	L2	CO2	5 M
	b)	Demonstrate a 3 x 8 decoder using 2 x 4 decoders and explain its operation as a minterm generator.	L3	CO2	5 M
		OR			

5	a)	Apply the following Boolean function using 8:1 multiplexer. $F(A,B,C) = \Sigma m(1,3,5,6)$	L3	CO2	5 M
	b)	Compare PROM, PAL, and PLA in terms of flexibility, hardware complexity, and applications.	L3	CO3	5 M
UNIT-III					
6	a)	Illustrate the logic circuit of JK master slave flip flop and explain its working with the truth table.	L3	CO3	5 M
	b)	Compare ring counter and Johnson counter with examples.	L2	CO3	5 M
OR					
7	a)	Demonstrate the truth table and state diagram of SR Flip Flop.	L2	CO3	5 M
	b)	Prepare a 3-bit asynchronous counter using JK flip-flops.	L3	CO3	5 M
UNIT-IV					
8	a)	Construct a Moore machine for a sequence detector that detects “110”.	L4	CO4	5 M
	b)	Analyze about sequential circuits, state table and state diagram.	L4	CO4	5 M
OR					

<table>
<tr><td>9</td><td>Determine the equivalence partition and reduced table for the given state machine shown in Table 1.
Table 1. State Machine
<table><tr><th rowspan="2">Present State</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr><tr><th>x = 0</th><th>x = 1</th><th>x = 0</th><th>x = 1</th></tr><tr><td>A</td><td>B</td><td>E</td><td>0</td><td>0</td></tr><tr><td>B</td><td>E</td><td>D</td><td>0</td><td>0</td></tr><tr><td>C</td><td>D</td><td>A</td><td>1</td><td>0</td></tr><tr><td>D</td><td>B</td><td>E</td><td>1</td><td>0</td></tr><tr><td>E</td><td>C</td><td>D</td><td>0</td><td>0</td></tr></table></td><td>L4</td><td>CO4</td><td>10 M</td></tr>
<tr><td colspan="6">UNIT-V</td></tr>
<tr><td rowspan="2">10</td><td>a)</td><td>Explain propagation delay with the help of input–output waveform diagrams.</td><td>L4</td><td>CO4</td><td>5 M</td></tr>
<tr><td>b)</td><td>Compare ECL, MOS and CMOS in terms of speed, power dissipation, and fan-out.</td><td>L2</td><td>CO4</td><td>5 M</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td rowspan="2">11</td><td>a)</td><td>Explain the working operation of Emitter Coupled Logic circuit.</td><td>L4</td><td>CO4</td><td>5 M</td></tr>
<tr><td>b)</td><td>Discuss the operation of CMOS logic circuits and list any two advantages.</td><td>L2</td><td>CO4</td><td>5 M</td></tr>
</table>