Code: 23EC3302

II B.Tech - I Semester – Regular Examinations - DECEMBER 2024

SWITCHING THEORY AND LOGIC DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours   Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
  2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
  3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
  4. All parts of Question paper must be answered in one place.

BL – Blooms Level   CO – Course Outcome

PART – A

		BL	CO
1.a)	Define Self Complimenting Code.	L1	CO1
1.b)	Simplify the following Boolean expression $F = A+B+A'B'C$.	L2	CO3
1.c)	Given $F = xy + x'z$. Convert this into canonical SOP form.	L2	CO3
1.d)	Realize Ex-OR gate using NAND Gates.	L3	CO2
1.e)	Draw the logic diagram of 4x1 Mux.	L2	CO2
1.f)	Write the truth table of BCD to 7-segment decoder.	L2	CO4
1.g)	Compare Latch and flip-flop.	L2	CO4
1.h)	Compare combinational and sequential circuits.	L2	CO4
1.i)	What is Mealy and Moore model?	L1	CO5
1.j)	Write the excitation table of JK flip-flop.	L1	CO5

PART – B

			BL	CO	Max. Marks
		UNIT-I			
2	a)	Using Hamming Code, the received message is 0001110. Find errors, if any, and give the correct message by using Even Parity.	L3	CO1	5 M
	b)	Perform BCD Subtraction for following decimal numbers: 56 - 28.	L3	CO1	5 M
		OR			
3	a)	Realise F = BD' + C'D' + B'D using NAND gates.	L2	CO2	5 M
	b)	Define Signed Binary number and explain the different compliment forms in signed numbers with example.	L2	CO1	5 M
		UNIT-II			
4	a)	Simplify F(A,B,C,D)=∑m(4,5,6,7,12,13,14)+d(1,9,11,15) using K-map.	L3	CO3	6 M
	b)	Implement the following Boolean function F = WY+WXY+W'XY+WX+Z using NAND gates.	L3	CO2	4 M
		OR			
5	a)	Convert the given function to canonical POS form F = (A+B)(B+C)(A+C)	L3	CO3	5 M
	b)	Simplify the following Boolean function using K-map F(A,B,C,D) = ΠM(1,3,4,11,12,13,14,15)	L3	CO3	5 M

UNIT-III

6	a)	Design BCD to Excess-3 Code Converter.	L5	CO4	5 M
	b)	Design and explain a 4-bit binary parallel Adder / Subtractor.	L4	CO4	5 M

OR

7	a)	Realise the function $F(A, B, C, D) = \sum m\ (0, 1, 5, 6, 7, 10, 14)$ using an 8x1 multiplexer.	L3	CO4	5 M
	b)	Design Full adder and draw the logic diagram with help of simplified output expressions.	L4	CO4	5 M

UNIT-IV

8	a)	Explain the operation of Master slave J-K flip flop.	L3	CO4	5 M
	b)	Explain the operation of bidirectional shift register with the help of logic diagram.	L3	CO4	5 M

OR

9	a)	Draw and explain a 4-bit ring counter using D - flip flops	L4	CO4	5 M
	b)	Derive the Characteristic equation, Excitation table and State diagram of D-flipflop.	L3	CO4	5 M

UNIT-V

10	a)	Design a 1011 sequence detector and draw its logic diagram.	L5	CO5	6 M
	b)	Explain State Diagram and State table.	L2	CO5	4 M

<div align="center">

OR

</div>

11	a)	Using partitioning minimization procedure reduce the following state table:	L3	CO5	5 M
		(see table below)			
	b)	A sequential circuit has two JK flip-flops A and B. The flip-flop input functions are: $J_A=B$; $K_A=Bx$ $J_B=x$; $K_B=A \oplus x$ i) Draw the logic diagram of the circuit ii) Tabulate the state table iii) Draw the state diagram	L4	CO5	5 M

PS	NS X=0	NS X=1	Output Z
A	D	B	1
B	A	E	0
C	A	E	1
D	C	A	0
E	F	D	0
F	F	D	1