PVP 23

Code: 23ES1304

II B.Tech I Semester – Supplementary Examinations – APRIL 2026

DIGITAL LOGIC AND COMPUTER ORGANIZATION

(Common for CSE, IT)

Duration: 3 hours Max. Marks: 70

Note: 1. This question paper contains two Parts A and B.
2. Part-A contains 10 short answer questions. Each Question carries 2 Marks.
3. Part-B contains 5 essay questions with an internal choice from each unit. Each Question carries 10 marks.
4. All parts of Question paper must be answered in one place.

PART – A

1.a)	State and draw the logic symbol of an XOR gate.
1.b)	Simplify the Boolean function F(w, x, y, z)=Σ(4, 5, 6, 7, 12) with don't-care function d(w, x, y, z)=Σ(0, 8, 13) using K-Map
1.c)	Draw three-state buffer. Describe its states.
1.d)	Describe the sequential circuit block diagram.
1.e)	What are the fields commonly present in an instruction format?
1.f)	What is the role of correction in BCD addition?
1.g)	Differentiate between RAM and ROM.
1.h)	Define hit ratio in cache memory.
1.i)	What is the need for an input–output interface?
1.j)	What is DMA and why is it used?

PART – B

					Max. Marks
UNIT-I					
2	a)	How Binary Coded Decimal (BCD) differ with decimal code? Perform the 184 + 576 using BCD.			5 M
	b)	Find the complement of the Boolean function $F = \bar{A}B\bar{C} + \bar{A}\bar{B}C$			5 M
OR					
3	a)	Briefly explain the basic gates in digital design.			5 M
	b)	Simplify the following Boolean function and draw the logic diagram and truth table. $F = \bar{x}\,\bar{y}\,z + \bar{x}\,y\,z + x\,\bar{y}$			5 M
UNIT-II					
4	a)	With neat sketch explain four-bit adder-subtractor with suitable example.			5 M
	b)	Compare asynchronous (latch-based) and synchronous (clocked) flip-flops in detail.			5 M
OR					
5	a)	Describe priority encoder truth table and logic diagram.			5 M
	b)	Design a 4-bit synchronous down counter using JK flip-flops.			5 M
UNIT-III					
6	a)	Describe the control word in register organization.			5 M
	b)	Write a detailed note on decimal subtraction with an example.			5 M

		OR	
7	a)	Write the program to evaluate $X = (A + B) * (C - D)$ using one and zero address instruction.	5 M
	b)	Describe the working of a decimal adder with a neat diagram.	5 M
		UNIT-IV	
8	a)	Explain the concept of memory hierarchy in computer systems with a neat diagram.	5 M
	b)	Discuss the differences between various page replacement techniques.	5 M
		OR	
9	a)	Differentiate between RAM and ROM with examples and applications.	5 M
	b)	Discuss cache replacement policies with suitable examples.	5 M
		UNIT-V	
10	a)	Explain different types of peripheral devices with examples.	5 M
	b)	Explain polling and daisy-chaining methods for handling priority interrupts.	5 M
		OR	
11	a)	Discuss different modes of data transfer in computer systems.	5 M
	b)	Explain interrupt-driven I/O mode with block diagram and example.	5 M