P.V.P SIDDHARTHA INSTITUTE OF TECHNOLOGY (AUTONOMOUS)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Guest Lectures

Department OF ECE				
S. No.	Department	Title and dates of programmes	Resource Persons	participants
PERIOD FROM 01.7.2024 to 1.4.2025				
1	ECE	Opportunities for Higher Education, 24-07-2024	E. Ramarao Sr. Counselor & Marketing Trainer GLOBAL DEGREES EDUCATION Vijayawada	IVECE (105)
2	ECE	Artificial Intelligence based Speech Processing,16-08-2024	Anil Kumar Vuppala. Associate Professor, IIIT Hyderabad.	IIECE& IVECE(143)
3	ECE	Energy Efficient VLSI Circuit Design with CMOS Devices, 6-2-2025	Dr Ramesh Vaddi Associate Professor, Electronics and Communication Engineering SRM University Amaravati Andhra Pradesh	IIIECE
4	ECE	Circuits for energy efficient processing of Deep Neural Networks on AI Edge,6-2-2025	Dr V Udaya Sankar Assistant Professor, Electronics and Communication Engineering SRM University Amaravati Andhra Pradesh	IIIECE

PVP SIDDHARTHA INSTITUTE OF TECHNOLOGY
KANURU, VIJAYAWADA – 7.

Dept. of E.C.E.

GUEST LECTURES & SEMINARS COMMITTEE

Date: 24-07-2024

This is to inform all the concerned that an expert talk on "Opportunities for Higher Education "is being arranged by ECE Dept. with the details as under:

Topic: "Opportunities for Higher Education"

Speaker: E. Ramarao
Sr. Counselor & Marketing Trainer
GLOBAL DEGREES EDUCATION

Venue: **Room No.113 (Gnd Floor)**

Time & Date: **1.00 P.M , 24-07-2024**

Note: 1) Students of IVECE are required to attend without fail.

Faculty Co-ordinator,
Guest Lectures & Seminars Committee.

(Dr.C.Subba Rao)
PROF. & H.O.D.

HEAD
Electronics & Communication Engg. Dept.
PRASAD V.POTLURI
SIDDHARTHA INSTITUTE OF TECHNOLOGY
KANURU, VIJAYAWADA-520 007.

CC: 1. Notice Board.
2. Principal for Information.

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Dept. of E.C.E.

GUEST LECTURES & SEMINARS COMMITTEE

Date: 14-08-2024

This is to inform all the concerned that an expert talk on "Speech Processing "is being arranged by ECE Dept. with the details as under:

Topic: "Artificial Intelligence based Speech Processing"

Speaker: Anil Kumar Vuppala.
Associate Professor,
IIIT Hyderabad.

Venue: Auditorium

Time & Date: 10.30 A.M , 16-08-2024

Note: 1) Students of IIECE & IVECE are required to attend without fail.

Faculty Co-ordinator,
Guest Lectures & Seminars Committee.

(Dr.C.Subba Rao)
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Electronics & Communication Engg.
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GUEST LECTURES & SEMINARS COMMITTEE

Date: 5-02-2025

This is to inform all the concerned that an expert talk on "VLSI "is being arranged by ECE Dept. with the details as under:

Topic: "Energy Efficient VLSI Circuit Design with CMOS Devices,"

Speaker: Dr Ramesh Vaddi
Associate Professor,
Electronics and Communication Engineering
SRM University
Amaravati
Andhra Pradesh.

Venue: Embedded systems Lab

Time & Date: 10.00 A.M , 6-2-2025

Note: 1) Students of IIIECE are required to attend without fail.

Faculty Co-ordinator,
Guest Lectures & Seminars Committee.

(Dr.C.Subba Rao)
PROF. & H.O.D.

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Dept. of E.C.E.

GUEST LECTURES & SEMINARS COMMITTEE

Date: 5-02-2025

This is to inform all the concerned that an expert talk on "Neural Networks "is being arranged by ECE Dept. with the details as under:

Topic: "Circuits for energy efficient processing of Deep Neural Networks on AI Edge"

Speaker: Dr V Udaya Sankar
Assistant Professor,
Electronics and Communication Engineering
SRM University
Amaravati
Andhra Pradesh

Venue: Embedded systems Lab

Time & Date: 11.30 A.M , 6-2-2025

Note: 1) Students of IIIECE are required to attend without fail.

Faculty Co-ordinator,
Guest Lectures & Seminars Committee.

(Dr.C.Subba Rao)
PROF. & H.O.D.

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Electronics & Communication Engg.Dept.
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

WORKSHOPS

S. No.	Department	Title and dates of workshops	Resource Persons	participants
PERIOD FROM 01.07.2024 TO 1.4.2025				
1	ECE	One week workshop on PCB Design IIECE_ SI 27-8-24 to 02.09.2024 and IIECE_ S2 23.12.2024 to 28.12.2024	Program Coordinator:Haji Habibulla MD, Sr. Asst. Prof.,ECE Resource Person:Rubeena ,Trainer APSSDC	2nd year ECE students(142)
2	ECE	One day Workshop on GENAI: The New Normal, 18-07-2024	Uma Maheswar Desu, CEO of VV Creations, Vijayawada	Faculty & students (9 faculty and 115 IIIECE students)
3	ECE	A Two Day Workshop On Advanced Simulation Tools for E.C.E. Laboratories (In Association With IETE Vijayawada center), 20-9-2024 & 21-9-2024	Dr. C. Subba Rao Dr. Ch. Gangadhar Dr.T.Maha Lakshmi Mrs. L.Madhavi Devi Mrs. D.Praveena Bai	Technicians of Engineering colleges
4	ECE	A 5 Days Workshop on Digital System Design Using FPGA 17 -9- 2024 to 19 -9- 2024, 01-10-2024 &03 -10- 2024	Dr. Ch. Gangadhar Dr.T.Maha Lakshmi Mrs. D.Praveena Bai	IIIECE Students
5	ECE	Two days Training Program on Cadence VLSI Tools on 24-1-2025 & 25-1-2025	P.Rajendra Application Engineer Entuple Technologies, Bangalore	Faculty& IV ECE Students

DEPARTMENT OF ECE

P V P Siddhartha Institute of Technology

Vijayawada, AP - 520007

One day Workshop on

GENAI: The New Normal

(Coding is Dead)

Resource Person: Uma Maheswar Desu

CEO of VV Creations, Vijayawada

18-07-2024

09.00 AM

Venue: Room No: 113

Department of Electronics & Communication Engineering
(Accredited by NBA)
Prasad V. Potluri Siddhartha Institute of Technology
(Accredited by NAAC: A+)
Approved by AICTE New Delhi and Permanently Affiliated to JNTUK, Kakinada

A 5 Days Workshop on Digital System Design Using FPGA

Resource Persons :- Dr. Ch. Gangadhar
Dr. T. Mahalakshmi
Mrs. Praveena Bhai

No Registration Fee

- **Dates of Workshop:** 17 September 2024 - 19 September 2024, 01 October 2024 & 03 October 2024
- **Venue :-** VLSI LAB
- **Theme :-** Hands-on training with Spartan 3E FPGA evaluation boards can be an excellent way to learn about digital design and FPGA programming.
- **Intrested Students Send Their Details to this Email Id:** dasari.maha@pvpsiddhartha.ac.in

For any Quires Contact

Dr. Ch. Gangadhar
Cell: +91-9440577560

Prasad V Potluri Siddhartha Institute of Technology
(AUTONOMOUS) NAAC A+
Approved by AICTE and permanently affiliated to JNTUK

Two days Training Program on Cadence VLSI Tools on 24 & 25 January - 2025

Schedule for Two days Training Program on Cadence VLSI Tools

Day-1:(24-01-2025)

Session-1: (10 am - 12 pm)

Introduction to Semi-Custom IC Design Flow
Cadence Solutions for Semi-Custom IC Design
Functional Verification using Incisive
RTL Synthesis using Genus Synthesis Solution

Session-2: (2 pm - 4 pm)

Physical Implementation using Innovus that includes
✓Floor Planning ✓ Power Planning
✓Placement
✓ CTS✓ Routing
Timing Analysis
Power Analysis
Parasitic Extraction
Generation of GDSII

Day-2:(25-01-2025)

Session-1: (10 am - 12 pm)

Introduction to Full Custom IC Design Flow
Cadence Solutions for Custom IC Design
Schematic Capture using Virtuoso
Schematic Editor
Symbol Creation
Testbench Creation using Virtuoso
Schematic Editor
Functional Simulation using Spectre
Monte Carlo Simulation

Session-2: (2 pm - 4 pm)

Layout Design using Virtuoso Layout Editor
Physical Verification which includes DRC & LVS
Parasitic Extraction using Quantus
Post Layout Simulation
Generation of GDSII

ENTUPLE TECHNOLOGIES

Trainer : P.Rajendra (Application Engineer)
Venue : Embedded Lab
Room No : 357

Department of
Electronics and Communication Engineering

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A 5 Days Workshop
on
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