VLSI DESIGN

Course Code	20EE4701D	Year	IV	Semester	I
Course Category	Professional Elective-III	Branch	EEE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	D&AC
Continuous Internal Evaluation:	30	Semester End Evaluation:	70	Total Marks:	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Understand MOS transistor fabrication, design and testing processes. (L2)
CO2	Choose an appropriate knowledge on the Properties and testing processes of MOS Technologies. (L3)
CO3	Develop the layout of any logic circuit which helps to understand and estimate parasitic of any logic circuit. (L3).
CO4	Illustrate the Electrical Properties, testing processes of MOS and BiCMOS Circuits. (L4).
CO5	Analyze the different design process to build a circuit. (L4)
CO6	Ability to do various applications in VLSI circuits and submit a report.

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:High, 2: Medium, 1:Low)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1														
CO2	3							1					2	1
CO3	3		1		1								2	1
CO4		3					1					1	2	1
CO5		3				1							2	1
CO6									3	3	1			

SYLLABUS		
Unit No.	**Contents**	**Mapped CO**
I	Introduction to MOS Technology: Integrated Circuit (IC) Era, Metal-Oxide semiconductor (MOS) and related VLSI technology, basic MOS transistors, NMOS & CMOS fabrication, comparison of NMOS, CMOS, BICMOS, technologies. Electrical Properties of MOS circuits: Drain current vs Drain Source voltage relationships, MOS transistor threshold voltage, figure of merit-ω0 ,Transconductance-gm, gds,pass transistor, NMOS inverter, CMOS inverter	CO1,CO2 CO4 & CO6
II	**VLSI Circuit Design Processes:** MOS Layers, Stick Diagrams, Design Rules and Layout- Lambda(λ)-based design rules, contacts and Transistors Layout Diagrams, 2µm micron-based design rules.	CO1,CO3, CO5&CO6

III	**Gate level Design:** CMOS Logic gates and other complex gates, Some architectural issues, Switch Logic, Gate Logic**,** Time Delays, Driving large Capacitive Loads, Wiring Capacitances, Choice of layers.	CO1,CO3 CO5 &CO6
IV	**VLSI Design styles:** VLSI Design Flow, Implementation approach in VLSI design -Full-custom, Semicustom, Gate-arrays, FPGAs and CPLDs architecture, Standard Cell.	CO1,CO3, CO5&CO6
V	**CMOS Testing:** CMOS Testing, Need for Testing, Test Principles, Design Strategies for Test, Chip Level and Board Level Test Techniques.	CO1,CO2 CO4 & CO6

Learning Resources
Text Books:
1. Douglas A, Pucknell, Kamran Eshraghian "Essentials of VLSI circuits and systems", PHI,1st Edition ,2005 2. Neil H. E Weste, David Harris, "CMOS VLSI Design – A Circuits and Systems Perspective", Pearson ,3rd Edition, 2009.
Reference Books:
1. John .P. Uyemura,"CMOS logic circuit Design" - Springer, 2007. 2. Wayne Wolf "Modern VLSI Design System-on-Chip Design", Pearson Education, 3rd Edition, 1997. 3. K. Lal Kishore "VLSI Design",IK international publishing house.,2013
E-Resources: 1. https://nptel.ac.in/courses/108/107/108107129/ 2. http://swarm.cs.pub.ro/~mbarbulescu/SMPA/CMOS-VLSI-design.pdf