DSP PROCESSORS

Course Code	20EC4702E	Year	IV	Semester	I
Course Category	Professional Elective-V	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation:	30	Semester End Evaluation:	70	Total Marks:	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	**Comprehend** the concepts of digital signal processing techniques. (L2)
CO2	**Identify** various sources of errors. (L3)
CO3	**Illustrate** Architectural features of programmable DSP devices. (L3)
CO4	**Analyze** the performance of processor based on pipelining concepts. (L4)
CO5	**Develop** basic DSP algorithms using DSP Processors.(L3)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2
CO1	2									1			1	1
CO2	2									2			2	2
CO3	3									2			2	2
CO4		2								2			2	2
CO5	2									2			2	2
Average* (Rounded to nearest integer)	**2**	**2**								**2**			**2**	**2**

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**Computational accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.	CO1,CO2
II	**Architectures for Programmable DSP Devices**: Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.	CO1,CO3

III	**Execution Control and Pipelining:** Hardware looping, interrupts, stacks, relative branch support, pipelining and performance, pipeline depth, interlocking, branching effects, interrupt effects, pipeline programming models	CO1,CO 4
IV	**Programmable Digital Signal Processors**: Introduction, Commercial Digital Signal Processing devices, architecture of TMS320C54xx Digital Signal Processors, addressing modes of the TMS320C54xx processors, memory Spaces of TMS320C54xx processors, program control, TMS320C54xx instructions and programming, on Chip peripherals, interrupts, pipeline operation of the TMS320C54xx processors	CO1,CO 3
V	**Implementations of Basic DSP Algorithms & Interfacing:** Introduction, The Q-notation, FIR Filters, IIR Filters, interpolation filters, decimation filters, PID controller, adaptive filters, 2-D Signal Processing, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).	CO1,CO 5

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Learning Resources
Text Books
1. Avtar Singh, S.Srinivasan, Digital Signal Processing, Cengage Learning, 2004. 2. Phil Lapsley, DSP Processor Fundamentals: Architectures and Features, IEEE Press, 1997.
Reference Books
1. Sen M.Kuo, Real-Time Digital Signal Processing, 2nd Ed., Wiley Student Edition, 2010. 2. B.Venkata Ramani, M.Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, Tata McGraw Hill, 2004. 3. Jonatham Stein, Digital Signal Processing, Wiley Student Edition, 2005
e- Resources & other digital material
1. https://ocw.snu.ac.kr/node/25239 2. https://nptel.ac.in/courses/108106149