PVP SIDDHARTHA INSTITUTE OF TEHNOLOGY, KANURU, VIJAYAWADA
(AUTONOMOUS)
INFORMATION TECHNOLOGY

Computer Organization

Course Code	20IT3402	Year	II	Semester	II
Course Category	PC	Branch	IT	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	-
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100

Course Outcomes		
Upon successful completion of the course, the student will be able to		
CO1	Understand the basic functional units of a computer system and its organization.	L2
CO2	Apply appropriate instructions for processing various types of computer operations.	L3
CO3	Apply various types of organizations on registers.	L3
CO4	Analyze memory hierarchy, I/O communication and pipelining.	L4

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:Substantial, 2: Moderate, 1:Slight)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3												3	
CO2	3												3	
CO3	2								2	2			2	
CO4		3											3	

Syllabus		
Unit No	**Contents**	**Mapped CO**
I	**Register Transfer and Micro-Operations** Register Transfer Language, Register Transfer, memory Transfers, Bus construction with Multiplexers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit.	CO1,CO2
II	**Basic Computer Organization** Instruction codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input-Output and Interrupt.	CO1,CO2
III	**Central Processing Unit** General registers Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control.	CO1,CO2, CO3
IV	**Computer Arithmetic** Introduction, Addition and Subtraction, Booth Multiplication Algorithm. **Memory Organization** Memory Hierarchy, Main Memory, Auxiliary memory, Associative Memory, Cache Memory, Virtual Memory.	CO1,CO3
V	**Input-Output Organization** Peripheral Devices, Input-output Interface, Asynchronous Data Transfer, Priority Interrupt, Direct Memory Access (DMA), Input-Output Processor. **Pipeline and Parallel Processing** Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline.	CO1,CO4

Learning Resources
Text Books
1. *Computer System Architecture*, Morris M. Mano, Third Edition, 1992, Pearson.
References
1. *Computer Organization and Architecture*, William Stallings, Eighth Edition, 2010, PHI.   2. *Computer Organization*, Carl Hamachar, Vranesic, 2002, McGrawHill.
e- Resources and other Digital Material
1. https://nptel.ac.in/courses/106/106/106106092/