PVP-19

ASIC DESIGN

Course Code	19EC4602C	**Year**	III	**Semester**	II
Course Category	Program Elective-III	**Branch**	ECE	**Course Type**	Theory
Credits	3	**L-T-P**	3-0-0	**Prerequisites**	Digital Logic Design
Continuous Internal Evaluation:	30	**Semester End Evaluation:**	70	**Total Marks:**	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Describe the programming technologies of an ASIC and its construction (L2).
CO2	Design and simulation of digital ICs using Verilog (L5)
CO3	Compare different testing procedures for VLSI circuits. (L2)
CO4	Analyze the algorithms of partitioning, placement and routing (L4)

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	3		3		3					3			3	
CO2	3		3		3					3			3	
CO3	3	3								3			3	
CO4	3	3								3			3	
Average* (Rounded to nearest integer)	3	3	3	3	3					3			3	

Syllabus

Unit No.	Contents	Mapped CO
I	**Types of ASICs:** Full-Custom ASICs, Standard-cell-based ASICs, Gate array-based ASICs, channelled gate array, channel less gate array, structured gate array, programmable logic devices, field programmable gate arrays, design flow, case study. ASIC Cell Libraries. ASIC library design: transistors as resistors, transistor parasitic capacitance	CO1
II	**Verilog:** Basics of the Verilog language, operators, hierarchy, procedures and assignments, timing controls and delay, logic-gate modeling, modelling delay, altering parameters. **Logic Synthesis**: A logic-synthesis example, MULTIPLEXER, inside a logic synthesizer verilog and logic synthesis.	CO2
III	**Simulation:** Types of simulation, MUX example, logic systems, how logic simulation works, delay models, static timing analysis, switch-level simulation, transistor-level simulation.	CO2

IV	**Test:** The importance of test, boundary-scan test, faults, fault simulation, automatic test-pattern generation, scan test, built-in self-test, a simple test example.	CO3
V	**ASIC Construction:** Physical design, system partitioning, partitioning methods. **Floor planning and Placement**: Floor planning, placement, physical design flow, **Routing:** Global routing, detailed routing,	CO4

Learning Resources
Text Books
1. Michael John Sebastian Smith, Application-Specific Integrated Circuits, Pearson Education, 2001.
Reference Books
1. Jan. M. Rabaey, Digital Integrated Circuits, 2/e, Prentice Hall, 2001 2. Sabih Gerez, Algorithms for VLSI Design Automation, Wiley, 1999. 3. Wayne Wolf, Modern VLSI Design, 4/e, Pearson Education, 2002. 4. Samir Palnitkar, Verilog HDL, 2/e, Pearson Education, 2003