## **PVP-19**

## COMPUTER ORGANIZATION AND DESIGN

<b>Course Code</b>	19EC4501E	Year	III	Semester	Ι
Course Category	Program Elective-1	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation:	30	Semester End Evaluation:	70	Total Marks:	100

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	Course Outcomes
Upon	successful completion of the course, the student will be able to
CO1	Know the functional unit of the processor such as the register file and arithmetic
	logical unit and with the basic of system topic (L2)
CO2	Outline the sequence of instruction execution, concept of pipelining, and modes of
	data transfer. Analyse the CPU design including the RISC/CISC architectures (L3)
<b>CO3</b>	Demonstrate the basic knowledge of I/O devices and interfacing of I/O devices.
	(L2)
<b>CO4</b>	Analyse various issues related to memory hierarchy (L3)

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## Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

\* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	P07	PO8	PO9	PO1 0	PO1 1	PO 12	PSO 1	PSO 2
CO1	3	3	3										3	
CO2	3	3	3										3	
CO3	3	3	3										3	
CO4	3	3	3										3	
Average* (Rounded to nearest integer)	3	3	3										3	

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Unit No.	Contents	Mapped CO
Ι	<b>Register Transfer and Micro operations:</b> Register transfer language, register transfer, bus and memory transfer, arithmetic micro operations, logic micro operations, shift micro operations, arithmetic logic shift unit.	CO1
II	<b>Computer Description:</b> Instruction codes, computer registers, computer instructions, timing and control, instruction cycle, memory-reference instructions, input-output and interrupt.	CO2
III	<b>Micro programmed Control:</b> Control memory, address sequencing. Central Processing Unit: General register organization, stack organization, addressing modes, reduced instruction set computer (RISC).	CO2, CO3

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IV	Input-Output Organization: Peripheral devices, input-output CO1,CO3						
	interface, modes of data transfer, direct memory access.						
V	Memory Organization: Memory hierarchy, main memory, cache CO1, CO4						
	memory, virtual memory.						
	Learning Resources						
Text I	Books						
1.	Morris Mano, Computer System Architecture, 3/e, Pearson Education, 2000.						
Refer	ence Books						
1.	William Stallings, Computer Organization and Architecture, 6/e, Pearson						
	Education Asia, 2000.						
2.	David A. Patterson, John L. Hennessy, Computer Organization and Design: The						
	hardware / software interface, 3/e, Morgan Kaufmann, 2002.						
3.	John P. Hayes, Computer Architecture and Organization, 3/e, McGraw-Hill,						
	1998.						
e- Res	sources & other digital material						
1.	http://nptel.iitm.ac.in/courses/Webcourse-contents/IITKANPUR/Comp						
	Architecture/page1.htm						
2.	http://nptel.iitm.ac.in/courses/Webcourse-contents/IIT20Guwahati/comp_org_arc						
	web/index.htm						