## **DIGITAL SYSTEM DESIGN**

<b>Course Code</b>	19EC4501C	Year	III	Semester	I
Course	Program	Branch	ECE	Course Type	Theory
Category	Elective-I				
Credits	3	L-T-P	3-0-0	Prerequisites	Digital Logic
					Design
Continuous	30	Semester	70	<b>Total Marks:</b>	100
Internal		End			
<b>Evaluation:</b>		<b>Evaluation:</b>			

Course Outcomes					
Upon successful completion of the course, the student will be able to					
CO1	Understand Memories and Programmable Logic Devices (L2).				
CO2	Analyze algorithmic state machines and asynchronous sequential circuits (L4).				
CO3	Design logic gates using different logic families(L5)				
CO4	Impart the basics of functional verification languages (L2)				

Mapping of course outcomes with Program outcomes (CO/ PO/PSO Matrix)

Note: 1- Weak correlation 2-Medium correlation 3-Strong correlation

\* - Average value indicates course correlation strength with mapped PO

COs	PO1	PO2	PO3	PO4	PO5	PO6	<b>PO7</b>	PO8	PO9	PO10	PO11	PO 12	PSO 1	PSO 2
CO1	3		3		3					3			3	
CO2	3		3		3					3			3	
CO3	3	3								3			3	
CO4	3	3								3			3	
Average* (Rounded to nearest integer)	3	3	3	3	3					3			3	

	Syllabus					
Unit No.	Contents	Mapped CO				
I	MEMORY AND PROGRAMMABLE LOGIC: Introduction, Random Access Memory, Memory Decoding, Error Detection and Correction, Read-Only Memory, Programmable Logic Array,	CO1				
II	Programmable Array Logic.  DESIGN AT THE REGISTER TRANSFER LEVEL: Introduction, Register Transfer Level (RTL) Notation, RTL Descriptions, Algorithmic State Machines(ASMs), Design Example (ASMD CHART), HDL Description of Design Example, Sequential Binary Multiplier, Control Logic, HDL Description of Binary Multiplier, Design with Multiplexers, Race-Free Design, Latch-Free Design.	CO2				
III	ASYNCHRONOUS SEQUENTIAL LOGIC: Introduction, Analysis Procedure, Circuits with Latches, Design Procedure, Reduction of state and flow tables, Hazards, Design Example.	CO2				

IV	DIGITAL INTEGRATED CIRCUITS: Introduction, Special	CO3						
	Characteristics, Bipolar-Transistor Characteristics, RTL and DTL							
	circuits, Transistor-Transistor Logic, Emitter Coupled Logic,							
	Metal-Oxide Semiconductor, Complementary MOS, CMOS							
	Transmission Gate circuits.							
V	SYSTEM VERILOG INTRODUCTION: System Verilog	CO4						
	Origins-The Accellera System Verilog Standard, Donations to							
	System Verilog, Key System Verilog enhancements for hardware							
	design.							

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## Text Books 1. Digital Design-M. Morris Mano, Michael D.Ciletti-6<sup>th</sup> Edition, Pearson Publishers 2. System Verilog for Design- Stuart Sutherland, Simon Davidmann, Peter Flake Refer → Books 1. Digital Design- John F.Wakerly- 4<sup>th</sup> Edition, PHI

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