PVP-19

DSP PROCESSORS AND APPLICATIONS

Course Code	19EC4501B	Year	III	Semester	I
Course Category	Program Elective - I	Branch	ECE	Course Type	Theory
Credits	3	L-T-P	3-0-0	Prerequisites	Nil
Continuous Internal Evaluation	30	Semester End Evaluation	70	Total Marks	100

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	Develop the Computational Accuracies in DSP implementation. (L3)
CO2	Demonstrate Architectures for different DSP devices. (L2)
CO3	Evaluate different pipelining concepts. (L5)
CO4	Classify different DSP Processors.(L4)
CO5	Interpret different DSP algorithms. (L2)

Contribution of Course Out comes towards achievement of Program Outcomes & Strength of correlations (3: High, 2: Medium, 1: Low)														
Cos	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO1	3	3	2	2	2							2	2	1
CO2	3	3	3	2	2							2	2	1
CO3	3	3	2	2	2							2	2	1
CO4	3	3	3	2	2							2	2	1
CO5	3	3	2	2	2							2	2	1
Average* (Rounded to nearest integer)	3	3	3	2	2							2	2	1

Syllabus		
Unit No.	**Contents**	**Mapped CO**
I	**Computational Accuracy in DSP Implementations:** Number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of error in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors, compensating filter.	CO1
II	**Architectures for Programmable DSP Devices:** Basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.	CO2
III	**Execution Control and Pipelining:** Hardware looping, interrupts, stacks, relative branch support, pipelining and performance, pipeline depth, interlocking, branching effects, interrupt effects, pipeline programming models	CO3

IV	**Programmable Digital Signal Processors:** Commercial digital signal processing devices, data addressing modes of TMS320C54XX processors, memory space, program control, instructions and programming, on-chip peripherals, interrupts and pipeline operation of TMS320C54XX processors.	CO4
V	**Implementations of Basic DSP Algorithms & Interfacing:** The Q-notation, FIR Filters, IIR Filters, interpolation filters, decimation filters, Computation of the signal spectrum, Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).	CO5

Learning Resources
Text Books
1. Avtar Singh, S.Srinivasan, Digital Signal Processing, Cengage Learning, 2004. 2. Phil Lapsley, DSP Processor Fundamentals: Architectures and Features, IEEE Press, 1997.
Reference Books
1. Sen M.Kuo, Real-Time Digital Signal Processing, 2/e, Wiley Student Edition, 2010. 2. B.Venkata Ramani, M.Bhaskar, Digital Signal Processors, Architecture, Programming and Applications, Tata McGraw Hill, 2004. 3. 3.Jonatham Stein, Digital Signal Processing, Wiley Student Edition, 2005