PVP 20

Code: 20ES1306

II B.Tech - I Semester – Regular Examinations - DECEMBER 2023

COMPUTER ORGANIZATION

(Common for AIML, DS)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	List the shift micro operations and explain each in detail.	L2	CO1	7 M
	b)	Construct 4-bit binary adder with neat diagram.	L3	CO3	7 M
OR					
2	a)	Explain 4-bit combinational circuit shifter with neat diagram.	L2	CO1	7 M
	b)	Construct a 4-bit combinational circuit decrementer using four full-adder circuits.	L3	CO3	7 M
UNIT-II					
3	a)	List and explain the significance of Registers of the basic computer in detail.	L2	CO1	7 M
	b)	Illustrate in detail about Input-Output instructions.	L3	CO2	7 M
OR					

4	a)	What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?	L2	CO1	7 M
	b)	Demonstrate the control gates associated with program counter (PC) in the basic computer.	L3	CO2	7 M
		UNIT-III			
5		What is an addressing mode? Explain the various addressing modes with suitable examples.	L2	CO1	14 M
		OR			
6		Assume yourself as a computer architect at TCS; you are assigned to compute the following arithmetic expression in assembly language using three, two, one, and zero address instruction formats. Y= (M + N/Z) * J - (P - Q) * (R + S).	L2	CO1	14 M
		UNIT-IV			
7	a)	One of the leading manufacturers of cache memory got feedback from the customers that the performance of their cache memories is not up to the mark. The manufacturing company assigned a team of experts to improve the performance of it. Here what are various possibilities the	L2	CO1	7 M

		experts will consider to improve the performance of cache memory? Explain these possibilities clearly with neat diagrams.			
	b)	Assume 5-bit registers that hold signed numbers (+15) X (-13), multiplication process using Booth Algorithm.	L4	CO4	7 M
		OR			
8	a)	Perform the operation (-9) + (-6) = -15, with binary numbers in signed -1's complement representation using only five bits to represent each number (including the sign).	L2	CO1	7 M
	b)	Consider the scenario given: 64-KB cache having 128-byte lines, It is a 4- way set-associative cache. The system uses a 32-bit address. Calculate the following: i) How many lines and sets do the cache have? ii) How many entries will be there in the tag? iii) How many bits of the tag is required in each entry in the tag?	L4	CO4	7 M
		UNIT-V			
9	a)	Consider a scenario in which you are appointed as a computer system analyst. Discuss direct memory access (DMA), the interface transfers data into and out of the memory.	L2	CO1	7 M

	b)	A processor manufacturing company decided to improve the number of instructions executed in a moment of time for their processor. A team of engineers in the company is started doing this job. They found that the clock period decreases while the number of pipeline stages increases in a processor. Discuss the various reasons a typical processor does not have hundreds/thousands of pipeline stages for the execution of the machine instructions.	L4	CO4	7 M
OR					
10	a)	Consider the following Assembly language code ***Sub*** R2, R1, R3 ***And*** R12, R2, R5. ***Or*** R13, R6, R2. ***Add*** R14, R2, R2. Identify the type of dependency and the hazards encountered for the above assembly language code.	L2	CO1	7 M
	b)	A computer architect is analyzing the function of various architectures such as SISD, SIMD, MISD, and MIMD. Discuss the main differences the architect found from these four architectures.	L4	CO4	7 M